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GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING FOR WOMEN
(AUTONOMOUS)
(Affiliated to Andhra University, Visakhapatnam)
B.Tech. - I Semester Regular / Supplementary Examinations, January – 2026
ELEMENTS OF ELECTRONICS ENGINEERING
(CSE-AI&ML)

1. All questions carry equal marks
2. Must answer all parts of the question at one place

Time: 3Hrs. **Max Marks: 70**

UNIT-I

1. a. Explain the energy band theory of solids and classify materials into conductors, semiconductors, and insulators with neat diagrams. [7M]
   b. Discuss the role of doping in modifying carrier concentration of semiconductors. [7M]

OR

2. a. Derive the expression for diffusion current density in semiconductors. [7M]
   b Explain why mobility of electrons is higher than that of holes in semiconductors. [7M]

UNIT-II

3. a. With neat diagrams, explain the working of a Schottky diode and highlight its advantages over PN diode . [7M]
   b. A half-wave rectifier supplies a DC output of 5 V to a 500 Ω load. Calculate the DC current and rectifier efficiency. [7M]

OR

4. a. With a neat circuit diagram and explain half-wave rectifier with capacitor filter. [7M]
   b. Define ripple factor and efficiency of rectifiers. Compare half-wave and full-wave rectifiers. [7M]

UNIT-III

5 a. Explain the construction and working principle of PNP and NPN transistors with neat diagrams. [7M]
   b. Draw the input and output characteristics of a CE configuration and explain the different regions of operation (active, saturation, cutoff). [7M]

OR

6 a. With neat diagrams, explain the voltage divider bias circuit and show how it improves thermal stability compared to fixed bias. [7M]
   b. Define thermal runaway in BJTs. Explain the causes and methods used to prevent it in practical biasing circuits. [7M]

UNIT-IV

7 a. Draw the small-signal equivalent circuit of a CE amplifier and derive expressions for voltage gain and input resistance. [7M]

b. Sketch the frequency response curve of a transistor amplifier and explain the significance of bandwidth in communication systems. [7M]

OR

8 a. Compare CE, CB and CC amplifiers. [7M]

b. What is the need for multi-stage amplifier and explain the circuit of Two-stage RC coupled amplifier. [7M]

UNIT-V

9 a. A JFET has $I_{DSS} = 8$ mA and $V_P = -5$ V. Calculate I_D when $V_{GS} = -2$ V. [7M]

b. Explain the construction and transfer characteristics of depletion-mode MOSFET [7M]

OR

10 a. Explain the advantages of FETs over BJTs in terms of input impedance and noise performance [7M]

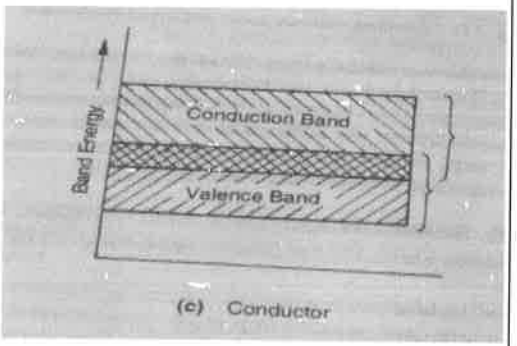
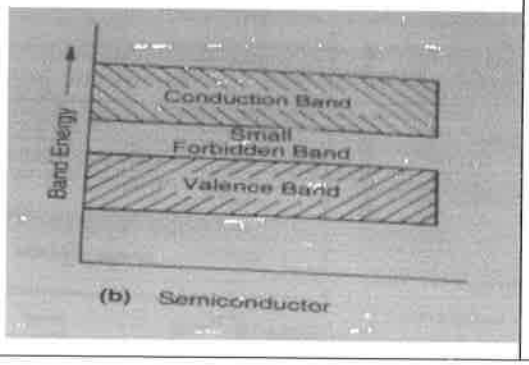
b. Compare the drain characteristics of enhancement-mode and depletion-mode MOSFETs. Discuss their applications in digital and analog circuits. [7M]

Gayatri Vidya Parishad College of Engineering for Women (Autonomous)
Madhurawada, Visakhapatnam
Department of Electronics & Communication Engineering
I B.Tech. I Semester – Sem Examination

Subject Name: Elements Of Electronics Engineering **Max. Marks:70M**

Faculty Name : Ms.L.Sarika **Branch&Section:CSM**

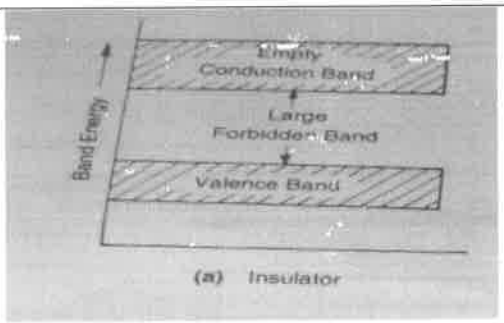
SCHEME OF VALUATION

Q.No	Description	Marks
1.a	**Energy Band Theory of Solids** In an isolated atom, electrons occupy discrete energy levels corresponding to different shells (K, L, M, etc.). These energy levels are well separated because the atom is not influenced by neighbouring atoms. A set of closely packed energy levels is called an **energy band**. **Valence Band, Conduction Band and Forbidden Energy Gap** 1. **Valence Band (VB):** ○ It is the **highest occupied energy band** at absolute zero temperature (0 K). ○ Contains valence electrons which are bound to atoms. ○ Electrons in this band generally **do not contribute to conduction**. 2. **Conduction Band (CB):** ○ It is the energy band **above the valence band**. ○ Electrons in this band are **free to move** and hence contribute to electrical conduction. ○ At 0 K, this band may be empty or partially filled depending on the material. 3. **Forbidden Energy Gap (Eg):** ○ The energy gap between the valence band and the conduction band. ○ No electron states are allowed in this region. ○ The width of this gap determines whether a material is a **conductor, semiconductor, or insulator**. **Classification of Materials Based on Energy Band Theory** **1. Conductors** • Valence band and conduction band **overlap**, or the conduction band is **partially filled**. • **Forbidden energy gap ≈ 0 eV**. • A large number of free electrons are available even at room temperature. • Hence, conductors have **high electrical conductivity**. **Examples:** Copper, Aluminium, Silver.  (c) Conductor **2. Semiconductors** • Valence band is **completely filled** at 0 K. • Conduction band is **empty** at 0 K. • A **small forbidden energy gap** exists between VB and CB. • **Eg ≈ 0.7 eV (Ge), 1.1 eV (Si)**. • At room temperature, some electrons gain thermal energy and jump from the valence band to the conduction band. **Examples:** Silicon, Germanium.  (b) Semiconductor	7M

3. Insulators

- Valence band is **completely filled**.
- Conduction band is **completely empty**.
- A **large forbidden energy gap** exists.
- **Eg > 3 eV**.
- Electrons cannot cross the forbidden gap under normal conditions.
- Hence, insulators have **very low conductivity**.

Examples: Glass, Rubber, Mica, Diamond.



1.b

Doping is the process of introducing impurities into a semiconductor material to modify its electrical properties. The role of doping is crucial in controlling the carrier concentration, which is essential for creating semiconductor devices.

Intrinsic Semiconductors- Pure semiconductors have equal numbers of electrons and holes (intrinsic carriers).
- The carrier concentration is determined by the temperature and the bandgap energy.

Doping- N-type doping: Introducing donor impurities (e.g., phosphorus) with an extra electron, increasing the electron concentration.
- P-type doping: Introducing acceptor impurities (e.g., boron) with a deficiency of electrons, increasing the hole concentration.

Effect of Doping on Carrier Concentration- Doping introduces additional energy levels within the bandgap, allowing for increased carrier concentration.
- The type and amount of doping determine the majority and minority carrier concentrations.

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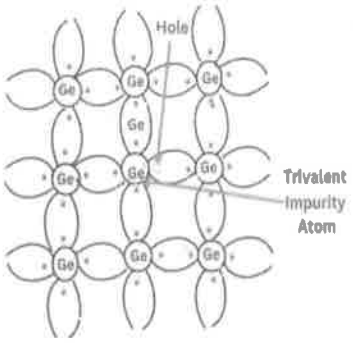
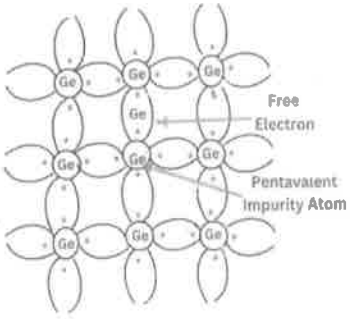
Importance of Doping- Allows for the creation of p-n junctions, the building blocks of semiconductor devices.
- Enables the control of electrical properties, such as conductivity and carrier mobility.
- Essential for the fabrication of various semiconductor devices, including transistors, diodes, and solar cells.

Formation of P-type semiconductor



Formation of N-type semiconductor



2.a

DIFFUSION CURRENT

- It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage provided a concentration gradient exists in the material.
- A concentration gradient exists if the number of either elements or holes is greater in one region of a semiconductor as compared to the rest of the Region.

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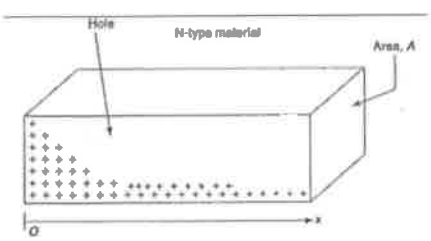
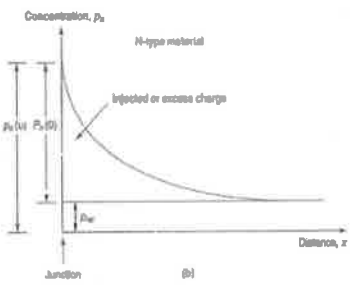




(a) Excess hole concentration varying along the axis in an N-type semiconductor bar
(b) The resulting diffusion current

→ In a semiconductor material the change carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers.
Thus the movement of charge carriers takes place resulting in a current called diffusion current.
The hole concentration p(x) in semiconductor bar varies from a high value to a low value along the x-axis and is constant in the y and z directions.
Diffusion current density due to holes Jp is given by $J_p = -qD_p \frac{dp}{dx}$ A/cm²

Since the hole density p(x) decreases with increasing x as shown in fig b, dp/dx is negative and the minus sign in equation is needed in order that Jp has positive sign in the positive x direction.
Diffusion current density due to the free electrons is given by

$$J_n = qD_n \frac{dn}{dx} \text{ A/cm}^2$$

Where dn/dx – concentration gradient for electrons
Dp/dx - concentration gradient for holes
Dn and Dp – diffusion coefficient for electrons and holes
The total current in a semiconductor is the sum of both drift and diffusion currents that is given by

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

$$J_n = qn\,\mu_n E + qD_n \frac{dn}{dx}$$

2.b

In semiconductor physics, mobility is a measure of how quickly a charge carrier can move through a crystal lattice when subjected to an electric field. In almost all common semiconductors (like Silicon and Germanium), the mobility of electrons is significantly higher than that of holes. 7M

There are three primary physical reasons for this disparity:

1. Effective Mass:The most fundamental reason is the difference in effective mass. In a crystal lattice, particles do not move as they would in a vacuum they interact with the periodic potential of the atoms.

   Mobility is inversely proportional to effective mass as shown below

   $$\mu = \frac{q\tau}{m^*}$$

   Where:

   - q is the electronic charge.
   - τ is the mean relaxation time (time between collisions).
   - m^* is the **effective mass**.

   Electrons in the conduction band generally have a much smaller effective mass than holes in the valence band.6 Because electrons are "lighter" in this context, they accelerate more quickly and move more easily under the same electric field.

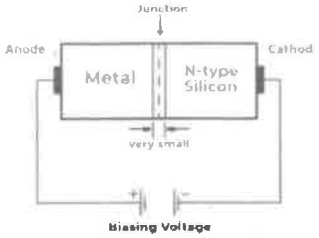
2. Band Structure and Energy States :The environment in which these carriers move is very different Conduction Band (Electrons):This band is mostly empty.Electrons move like "free" particles in a vast open space with very few obstacles or occupied states to block their path. Valence Band (Holes): This band is almost entirely full. For a hole to move, a valence electron must break a covalent bond and hop into a neighboring vacancy. This "hopping" process is inherently more restricted and slower than the movement of a free electron in the conduction band.

3. Scattering Mechanisms: Carrier mobility is also limited by how often a particle "bumps" into things (scattering).Holes are located in the valence band, which is closer to the nucleus of the atoms.They experience stronger electrostatic forces and more frequent interactions with the lattice ions.Electrons in the conduction band have higher energy and are further from the atomic nuclei, meaning they encounter less "resistance" or scattering from the internal atomic environment.

3.a

A Schottky diode is a type of diode with a metal-semiconductor junction instead of the typical semiconductor-semiconductor junction found in standard diodes. The Schottky diode has characteristics such as Low Forward Voltage Drop, Fast Switching Speed and other unique features that

make it more suitable for various applications such as
rectification, voltage clamping, voltage regulation, and RF detection.
Symbol of Schottky Diode

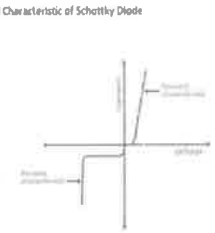


Working Of Schottky Diode

- When a metal contacts a semiconductor, a Schottky barrier is formed due to the difference in their work functions.
- This barrier initially restricts electron flow from the metal to the semiconductor.

Under forward bias (metal as anode, semiconductor as cathode), the applied voltage reduces the barrier height.
The reduced barrier allows easy electron flow, resulting in a low forward voltage drop (about 0.2–0.4 V for silicon).
Low forward voltage drop leads to low power dissipation, suitable for low-voltage applications.
Schottky diodes have very fast switching speed due to the absence of a depletion region like in PN junction diodes.
Hence, they are widely used in high-frequency and high-speed applications.
In reverse bias, a small leakage current flows due to thermionic emission of electrons over the Schottky barrier.

Advantages: Schottky diode has a lower forward voltage drop than a PN diode.
* It offers very fast switching speed.
* It has low power dissipation.
* It is suitable for high-frequency applications.
* It provides higher efficiency in low-voltage circuits.



3.b

Given DC output voltage $V_{DC} = 5$ V and load resistance $R_L = 500\,\Omega$.

The DC current is

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{5}{500} = 0.01\text{ A} = 10\text{ mA}$$

Rectifier efficiency is defined as

$$\eta = \frac{P_{DC}}{P_{AC}}$$

For a half wave rectifier,

$$I_{DC} = \frac{I_m}{\pi} \quad \text{and} \quad I_{rms} = \frac{I_m}{2}$$

$$P_{DC} = I_{DC}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$$

AC input power is

$$P_{AC} = I_{rms}^2 R_L = \left(\frac{I_m}{2}\right)^2 R_L$$

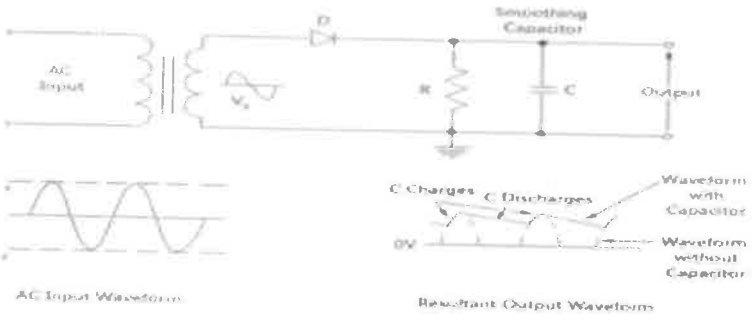
Therefore,

$$\eta = \frac{(I_m/\pi)^2 R_L}{(I_m/2)^2 R_L} = \frac{4}{\pi^2} = 0.406$$

Hence, the DC current is **10 mA** and the rectifier efficiency is **40.6% (maximum)**.

4.a **Operation:**

- During the positive quarter cycle of the AC input signal, the diode D is forward biased and it conducts. This quickly charges the capacitor C to the peak value of the input voltage VmV_mVm.
- When the input starts decreasing below its peak value, the capacitor remains charged at VmV_mVm and the ideal diode becomes reverse biased. This is because the capacitor voltage, which is the cathode voltage of the diode, becomes more positive than the anode. 7M
- During the negative half cycle and some part of the next positive half cycle, the capacitor discharges through RLR_LRL.
- The discharging of the capacitor is decided by the RLCR_L CRLC time constant, which is very large, and hence the capacitor discharges very little from VmV_mVm.
- In the next positive half cycle, when the input signal becomes more than the capacitor voltage, the diode again becomes forward biased and charges the capacitor back to VmV_mVm. The waveform is shown above.



4.b Definition of ripple factor : It is the ratio of the RMS value of the AC component present in the output to the average (DC) value of the output.

$$\gamma = \frac{V_{ac}}{V_{dc}} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$ 7M

Definition of efficiency : It is the ratio of the DC power output to the total AC power input.

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

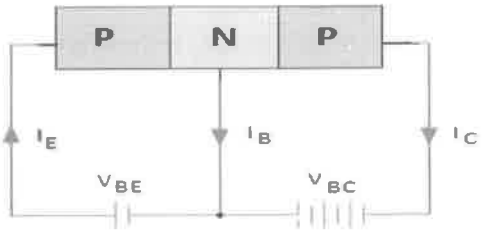
Comparision of half wave and full wave rectifiers:

Characteristic	Half-Wave Rectifier	Full-Wave Rectifier
Ripple Factor (γ)	**1.21** (High ripple)	**0.482** (Low ripple)
Max Efficiency (η_{max})	**40.6%**	**81.2%**
Form Factor	1.57	1.11
Output Frequency	f (same as input)	$2f$ (double input)

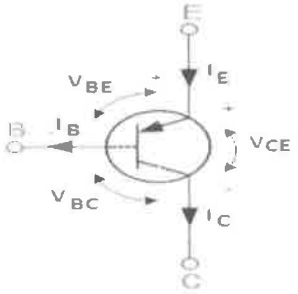
5.a **Construction of PNP Transistor**

A PNP transistor is built by sandwiching a layer of N-type semiconductors between two layers of P-type semiconductors. In comparison to the Base areas, the Emitter and Collector regions are highly doped. As a result, the depletion region at both junctions reaches the base region. The Emitter and Collector layers have a larger area than the base layer. Since, the middle layer is so thin and weakly doped, there are considerably fewer free electrons in the Base area. 7M

A PNP transistor consists of the three semiconductor layers:
Emitter: The outer layer is the P-type semiconductor material.
Base: The middle layer is N-type semiconductor material.
Collector: The innermost layer is also P-type semiconductor material.
These layers are typically arranged as P-N-P with the N-type base layer sandwiched between P-type emitter and collector layers.



Construction



Circuit Symbol

$I_C = I_E - I_B$

Working of PNP Transistor

The operation of a PNP transistor is based on the control of current flow between the emitter and collector by the current flowing into the base. Here's a brief overview:

When a positive voltage is applied to base-emitter junction. it allows the flow of electrons from emitter to the base.The flow of electrons from the emitter to the base creates a path for majority charge carriers to flow from collector to the emitter.

Construction of NPN transistor:

The NPN transistor is supported by three layers, two of which are P-type transistors and the other two of which are N-type transistors. While it's often simplistically described as semiconductors are formed by connecting two diodes sequentially, this analogy is primarily for conceptual understanding rather than an exact representation of the transistor's structure.

NPN-Transistor

Common Emitter Configuration

As a result, there are always three layers: the first is lightly doped, like base, the second is heavily doped, like Collector, and the third is Emitter, which is decently doped.

The Collector and Emitter of the P-type are sandwiched between the foundation of the N-type. As a result, a transistor of the N-type is created.

The emitter, base, and collector are the three layers that make up an NPN transistor.

Working of NPN Transistor

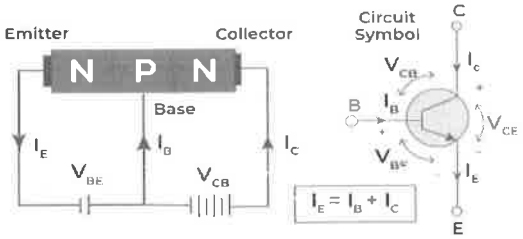
Forward bias should be used at the base-emitter junction, and reverse bias should be used at the collector base intersection. As a result, the negative terminal of the VBE is linked to the N-terminal of the emitter-base intersection, and the positive terminal of the battery is linked to the P-terminal of the VBE.

The N-terminal is connected to the VCB's positive terminal to invert the authority base intersection, while the P-terminal is connected to the battery VCE's negative terminal. As a result, the gatherer base intersection will have a wide exhaustion layer and the emitter base intersection will have a limited consumption layer.

A few electrons and holes will recombine due to the absence of many holes in the base region. Various electrons that have not yet recombined will move toward the gatherer district.

This will include the circuit's current. Because of its enormous size, the gatherer can dissipate heat and gather additional charge transporters. Since electrons are the primary charge transporters in the NPN transistor, the current is caused by electrons. The emitter current in an NPN semiconductor is equivalent to the amount of base and gatherer current. Numerically it tends to be composed as:

IE = IB + IC

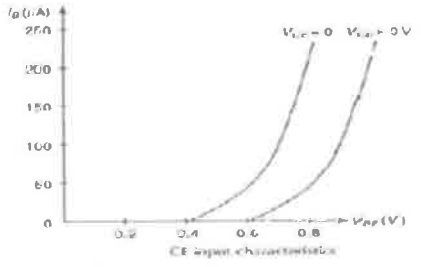


5.b **Input characteristics (CE configuration):**

Cut-off region: Base–emitter junction is not forward biased, base current

Active region: Base–emitter junction is forward biased, base current increases rapidly with base–emitter voltage

Saturation region: Base–emitter junction is strongly forward biased, further increase in base emitter voltage causes large base current but transistor approaches saturation.



CE input characteristics

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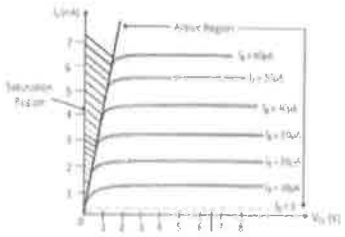
Output characteristics (CE configuration):

Cut-off region: Base current =0, collector current transistor Ic~0 is OFF
Active region: Base–emitter junction is forward biased and collector–base junction is reverse biased, used for amplification.
Saturation region: Both junctions are forward biased , is maximum and nearly independent of transistor is fully ON.



6.a **Voltage Divider Bias Circuit :**

A voltage divider bias circuit provides a stable operating point for a transistor by using two resistors connected across the power supply to create a fixed voltage at the base. This base voltage sets the condition for current to flow from the collector to the emitter.

Working :

The emitter is connected to ground through a resistor, which creates a feedback effect: if the current tries to increase, the voltage across this emitter resistor also increases, reducing the base-emitter voltage and automatically limiting the current. This self-adjusting action keeps the transistor's operating point stable, even if temperature changes or transistor properties vary.

Because of this design, the circuit maintains consistent performance and is widely used in amplifier applications where stability is important.

The voltage divider bias circuit improves thermal stability compared to fixed bias in several ways:

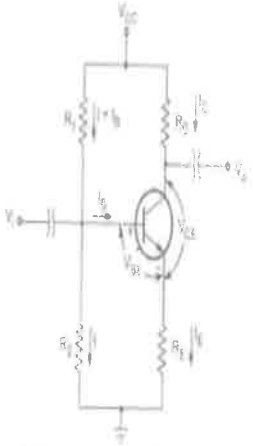


Fig. Voltage divider bias circuit

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- The base voltage is set by the voltage divider network, which is independent of the transistor's beta (current gain) and base-emitter voltage (VBE). This means that changes in temperature, which affect beta and VBE, have a minimal impact on the base voltage
- The emitter resistor provides negative feedback, which counteracts changes in the collector current. If the collector current increases due to temperature, the voltage across the emitter resistor also increases, reducing the base-emitter voltage and limiting the collector current.
- This self-regulating mechanism keeps the operating point stable, reducing the risk of thermal runaway and ensuring consistent performance.

6.b

Thermal runaway in a Bipolar Junction Transistor (BJT) is a condition in which an increase in junction temperature causes an increase in collector current, which further increases power dissipation and temperature, leading to uncontrolled rise in current and eventual destruction of the transistor.

Causes of Thermal Runaway

1. Increase in Collector Leakage Current
   Leakage current approximately doubles for every 10°C rise in temperature.
   $Ic=\beta Ib+(1+\beta)Icbo$
   This causes further heating.
2. Reduction in Base–Emitter Voltage
   Vbe decreases by about 2 mV/°C with temperature rise.
   Reduced Vbe increases base current, leading to higher collector current.
3. Increase in Power Dissipation
   Increase in ICI_CIC raises power dissipation
   Higher power dissipation increases junction temperature further.

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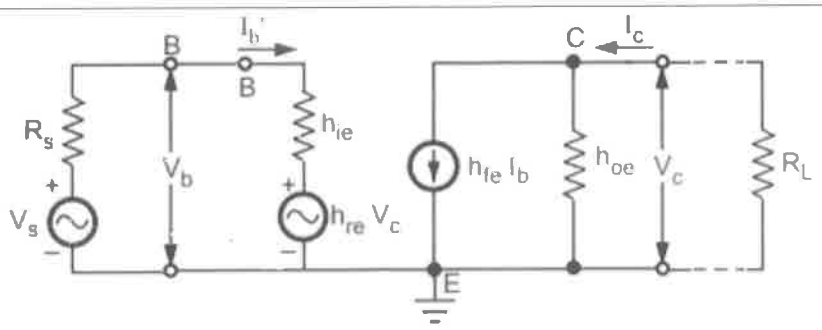
Methods to Prevent Thermal Runaway

1. Emitter Resistor (Negative Feedback)
   Adding an emitter resistor provides negative feedback.
   Increase in temperature Voltage Divider Bias Circuit
   Provides a fixed base voltage independent of β.
   Combined with emitter resistor, it offers excellent thermal stability.
2. Collector-to-Base Feedback Bias
   Increase in collector current reduces base current through feedback, limiting
3. Use of Heat Sinks
   Heat sinks dissipate excess heat, keeping junction temperature within safe limits.
4. Thermal Compensation Devices

Use of diodes, thermistors, or sensistors to compensate for temperature variations.

7.a



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Input resistance is defined as the ratio of input voltage to input current: $R_i = \frac{V_b}{i_b}$.

Step 1: Substitute the output relationship $V_c = -i_c R_L$ into the second h-parameter equation:

$$i_c = h_{fe} i_b + h_{oe}(-i_c R_L)$$

$$i_c(1 + h_{oe} R_L) = h_{fe} i_b \implies \frac{i_c}{i_b} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

Step 2: Substitute $V_c = -i_c R_L$ into the first h-parameter equation:

$$V_b = h_{ie} i_b + h_{re}(-i_c R_L)$$

$$V_b = h_{ie} i_b - h_{re} R_L \left(\frac{h_{fe} i_b}{1 + h_{oe} R_L} \right)$$

Step 3: Divide the entire expression by i_b:

$$R_i = \frac{V_b}{i_b} = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}$$

3. Derivation of Voltage Gain (A_v)

Voltage gain is the ratio of output voltage to input voltage: $A_v = \frac{V_c}{V_b}$.

Step 1: Express V_c in terms of i_b: From our previous step, $i_c = \frac{h_{fe} i_b}{1 + h_{oe} R_L}$. Since $V_c = -i_c R_L$:

$$V_c = -\left(\frac{h_{fe} i_b R_L}{1 + h_{oe} R_L} \right)$$

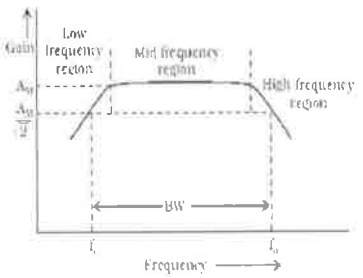
Step 2: Use the definition $A_v = \frac{V_c}{V_b} = \left(\frac{V_c}{i_b} \right) \cdot \left(\frac{i_b}{V_b} \right)$:

$$A_v = \left(\frac{-h_{fe} R_L}{1 + h_{oe} R_L} \right) \cdot \frac{1}{R_i}$$

7.b

Frequency regions:

1. Low-frequency region (f < fL):
   Gain decreases due to the effect of coupling capacitors and emitter bypass capacitor, whose reactance is high at low frequencies.
2. Mid-frequency region (fL < f < fH):
   Gain is maximum and constant. Capacitors act as short circuits and transistor operates normally. This is the useful operating region of the amplifier.
3. High-frequency region (f > fH):
   Gain decreases due to junction capacitances and Miller effect, which become significant at high frequencies

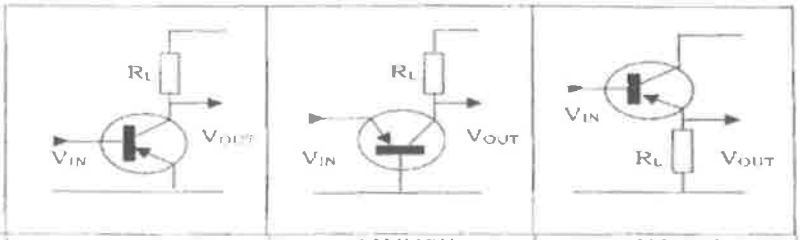


7M

Significance of bandwidth in communication systems:

1. Adequate bandwidth ensures faithful amplification of all frequency components of the signal.
2. Higher bandwidth allows higher data transmission rates, essential for modern communication systems.
3. Insufficient bandwidth causes signal distortion and loss of information.
4. Communication and RF amplifiers require wide bandwidth, while audio amplifiers need comparatively smaller bandwidth.

8.a



	COMMON EMITTER	COMMON BASE	COMMON COLLECTOR
CURRENT GAIN	20 to 200	< 1 (0.95 to 0.995)	20 to200
VOLTAGE GAIN	100 to 600	500 to 800	< 1
POWER GAIN	High	Medium	Low
INPUT IMPEDANCE	500 to 2000Ω	50 to 200Ω	20kΩ to 100kΩ
OUTPUT IMPEDANCE	10kΩ to 50kΩ	100kΩ to 1MΩ	20Ω to 500Ω
INPUT OUTPUT PHASE RELATIONSHIP	180° out of phase	In phase	In phase
TYPICAL USE	Normal amplifier	Impedance matching (low to high)	Impedance matching (high to low)

7M

0

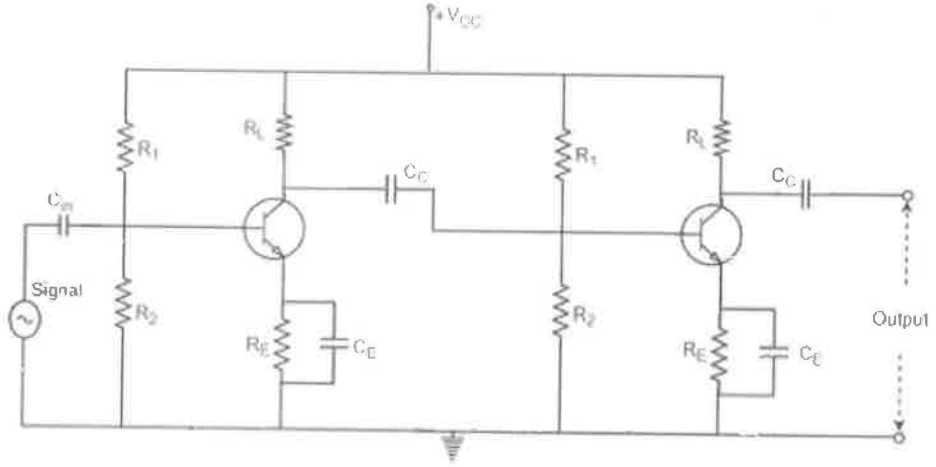
8.b **Multistage amplifier**

A multistage amplifier combines two or more single-stage amplifiers in cascade, where the output of one feeds the input of the next, to achieve much higher overall voltage, current, or power gain than a single stage can provide, using coupling devices (like capacitors or transformers) to connect stages and block DC bias.

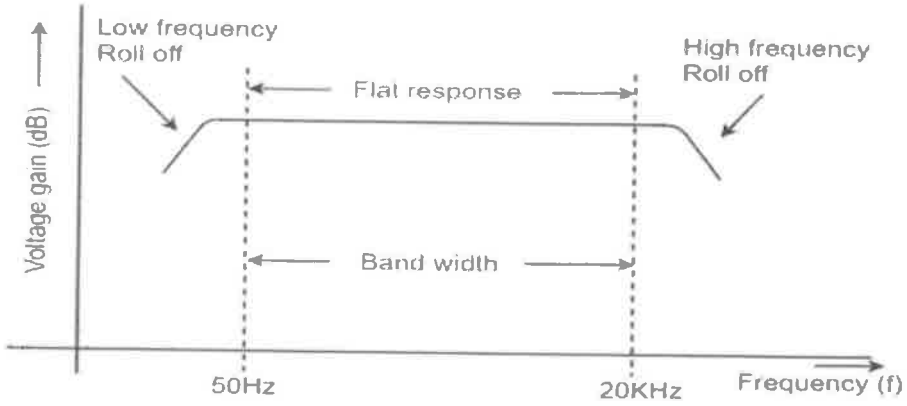
7M

Need for Multi-Stage Amplifier

1. **High Gain:** Multiple stages are used to amplify very weak signals to a usable level, since a single stage gives limited gain.
2. **Impedance Matching:** Input stage provides high input impedance and output stage provides low output impedance for efficient signal transfer.
3. **Power Amplification:** Early stages amplify voltage, while the final stage delivers sufficient power to drive the load.Diagram and its operation



Frequency response



9.a

Given:

Idss = 8 mA

Vp = −5 V

Vgs = −2 V

Formula:

$Id = Idss(1 - Vgs/Vp)^2$

Substitute the values in above equation:

$Id = 8(1 - (-2/-5))^2$ mA

$Id = 8(1 - 0.4)^2$

$Id = 8(0.6)^2$

$Id = 8 \times 0.36$

Id = 2.88 mA

7M

9.b

MOSFET is a transistor which is used as switch or amplifier and in many other applications. The basic construction of MOSFET can be explained as below:-

Substrate : MOSFET is constructed on a silicon wafer that is acts as a base of the device.

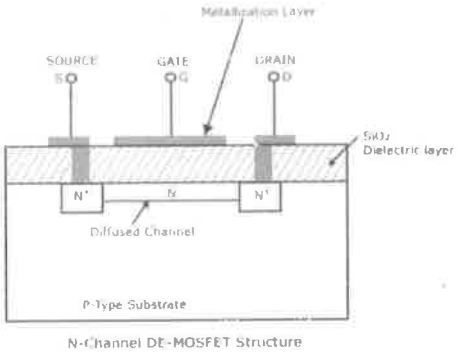
SiO2 : A thin layer of insulating material is formed with SiO2 for the exchange of electrons and holes.

Gate Terminal : A gate terminal is formed on the insulating layer. This controls the flow of current between the drain and source with the help of gate voltage.

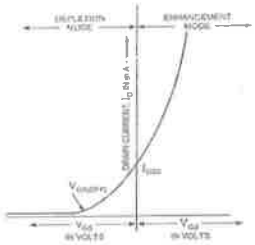
Source and drain terminals : These are created on the either side of the gate. These are basically doped regions.

Channel : Region between the gate, drain and source is known as channel which controls the flow of charge among them.

Transfer Characteristics : Id V/S Vgs for fixed VDS.



N-Channel DE-MOSFET Structure



7M

10.a

Advantages of FET over BJTs:

1. Higher Input Impedance
   - FETs are voltage-controlled devices, whereas BJTs are current-controlled devices.
   - In a FET, the gate draws negligible current (especially in JFETs and MOSFETs).
   - Therefore, FETs have very high input impedance:
     - JFET: 10^7-10^9Ω
     - MOSFET: 10^10-10^15 Ω
   - In contrast, BJTs require base current and have lower input impedance (typically a few kΩ).
2. Better Noise Performance
   - Noise in electronic devices mainly arises due to random motion of charge carriers.
   - In BJTs:
     - Conduction involves both electrons and holes.
     - Presence of base current introduces shot noise.
   - In FETs:
     - Conduction is due to only majority carriers.
     - No gate current → negligible shot noise.

7M

10.b

Drain Characteristics

Drain characteristics are the plots of drain current (Id) versus drain–source voltage (Vds) for different gate–source voltages (VGS).

Enhancement-mode MOSFET (E-MOSFET):

- Normally OFF at Vgs=0V
- Channel forms only when Vgs>Vtv
- Drain current starts flowing only after threshold voltage
- Used as a switch (clear ON/OFF behavior)

Depletion-mode MOSFET (D-MOSFET):

- Normally ON at Vgs=0V
- Channel already exists
- Negative Vgs reduces drain current, positive Vgs increases it
- Can operate in both depletion and enhancement regions

7M

Enhancement-Mode MOSFET Applications

Digital Applications:

- CMOS logic gates (NOT, NAND, NOR)
- Microprocessors and microcontrollers

Analog Applications:

- Power amplifiers
- Switching regulators

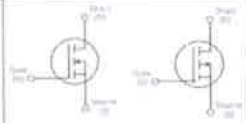
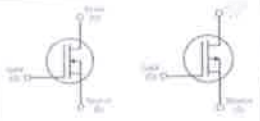
Depletion-Mode MOSFET Applications

Digital Applications:

- Load devices in NMOS logic
- Pull-up resistors in integrated circuits

Analog Applications:

- Constant current sources
- Voltage regulators

Sr. No.	Parameter	Enhancement MOSFET	Depletion MOSFET
1	**Operation**	Requires a positive gate voltage to conduct	Conducts in its natural state and requires no gate voltage
2	**Symbol**	 N Channel P Channel	 N Channel P Channel
3	**Threshold Voltage**	Positive threshold voltage required	Negative threshold voltage required
4	**Conductivity**	Normally off (non-conductive) in its natural state	Normally on (conductive) in its natural state
5	**Applications**	Widely used in digital circuits and CMOS technology	Less common in digital applications, more in analog circuits
6	**Carrier Type**	Majority carriers are electrons	Majority carriers are holes
7	**Voltage Biasing**	Commonly used in NMOS and PMOS transistors	Less commonly used in modern CMOS technology

Verified

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