M.MANI KUMARI

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OBJECTIVE:

To acquire a challenging and creative position in an esteemed organization by seeking exposure to latest technologies while making good contributions for further career development.

ACADEMIC QUALIFICATIONS:

S. No	Qualification	Board/University	College/School	Year of passing
1	PhD(Pursuing)	JNTU Kakinada	JNTU Kakinada	---
2	M.Tech (VLSI -D)	JNTU Kakinada	Shri Vishnu Engineering college,Bhimavaram	2010
3	B.Tech (ECE)	JNTU Hyderabad	Maharaj Gajapathi Raj College of Enginneing,Vizianagaram	2004
4	Diploma (ECE)	State Board of Technical Education AP,Hyderabad	Government Polytechnic for Women,Kakinada	2001
5	S.S.C	Board Of Secondary Education, AndhraPradesh	St.Johns High School,Amalapuram	1998

SKILL SETS:

Programming languages :	C, VHDL,Verilog
Operating systems :	MS-DOS, WINDOWS-98/XP/7/8/10

TEACHING EXPERIENCE:

S. No	Organization	Exp type	Experience	Designation	Experience	
					Years	Months
1	BVC Engineering College,Odalarevu	Academic	June-2004 to May-2006	Assistant Professor	2	0
2	Malla Reddy Enginnering College,Secunderabad	Academic	June-2006 to November-2008	Assistant Professor	2	08
3	Gayatri Engineering College for Women	Academic	December-210 to till date	Assistant Professor	9	0

SUBJECTS AT UNDERGRADUATE and POST GRADUATE LEVEL

Very High Speed IC Hardware Description Language	Algorithms for VLSI Design Automation
CMOS Mixed Signal Design	System on Chip Design
Digital IC Design	Digital IC Applications
Digital System Design& Digital IC Applications	System Design Through Verilog
Low Power VLSI Design	Electronic Circuit Analysis
Very Large Scale Integration	Switching Theory and Logic design

WORKSHOP

1. A two day National Level workshop on "**VLSI & EDA tools**" at JNTU Vizianagaram- **February 2014.**
2. A two day International Workshop on **"Cognitive Radio Technologies"** at GVPCEW-September-25,26 .
3. A three day International Workshop on "**Analog And Digital Circuit Design Using Cadence",** at GVPCOE(A),**9-11 December 2015**.
4. A three day International Workshop on **"Electro Magnetics &RF Fundamentals"** at GVPCEW **July- 2016**.
5. A two day Workshop on **"Recent Advancements In VLSI Technology And Design Using EDA Tools"** at **JNTU Kakinada during 24th to 26th June 2016.**
6. A two day hands on Workshop on "**VLSI design using EDA tools** , at GVPCEW
7. A two day national workshop on **"Signal Processing and Communication Systems",** at GVPCEW
8. A two weeks workshop on **"Mixed Signal and Radio Frequency VLSI Design"** 30 January to 14 February 2017 at GVPCE.
9. A two day national workshop on **"Custom Analog & Digital IC Design Using Mentor EDA Tools"** September 2018 at GVPCEW.

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ONLINE CERTIFICATION COURSES

1. A course on **"Switching Circuits & Logic design"** conducted by **NPTEL-AICTE** during **July-October 2018**.

PAPERS PUBLISHED

1. **"Bit Swapping LFSR and its Application to Fault Detection and Diagnosis Using FPGA"** International Journal of Engineering Research & Technology (IJERT) IJERT ISSN: 2278-0181 IJERTV2IS90472 www.ijert.org Vol2 Issue 9
2. **"Interconnect Delay and Power Optimization Using Schmitt Trigger as Alternate Approach to Buffer Insertion"**, International Journal Of Science and Research(IJSR),ISSN(online):2319-7064 Impact Facor(2012):3.358
3. **"Low Power and High Performance VLSI Interconnects By Schmitt Trigger Technique In Nano-scale Regime"** IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 5, Ver. II,October-2014.
4. **"Boostable Repeater Design with Dual Adaptive Supply Voltage for VLSI Interconnects".** International Journal of Advance Engineering and Research Development Volume 2,Issue 11,November 2015.
5. **"Dynamic Feedback Control 10T SRAM Cell"** International Journal of Applied Sciences, Engineering and management ISSN 2320- 3439,Vol-6 No-04,July-2017 PP 17-22.
6. **"Design and implementation of positive feedback comparator in terms of Power and Delay"** IOSR journal of VLSI & Signal Processing(IOSR-JVSP),Volume-9 Issue 4,Ser-I, July-August 2019 PP 10-17 e Issn:2319-4200 P ISSN N0:2319-4197.
7. **"SRAM Based Look Up Table Design Using Multiple Valued Logic"** Jour of Adv Research in Dynamical & Control Systems Vol-11,07-Special issue,2019.

CONFERENCES ATTENDED

1. **"Boostable Repeater Design with Dual level Adaptive Supply Voltage for Variation Resilience in VLI Inter connects"** at JNTU Kakinada Nov- 6,7 2015.
2. **"Design of Latched Comparator Using Multiple Valued Logic"** at JNTU Kakinada July-19,20 2018.

M.Tech PROJECTS GUIDED: 7

1.	Bit Swapping LFSR and its Application to Fault Detection and Diagnosis Using FPGA
2.	Low power and High performance in VLSI Interconnects by schimitt trigger technique in Nano scale regime
3.	Boostable repeater design with Dual adaptive supply voltage for VLSI Interconnects
4.	Implementation of Digital Circuits using Multiple Valued Logic
5.	Dynamic Feedback Control 10T SRAM Cell
6.	SRAM Based Look Up Table Design Using Multiple Valued Logic
7.	Design and Implementatin of Positive Feedback Comparator interms of Power and Delay

B.Tech PROJECTS GUIDED

1.	Implementation of Low power Column by pass Multiplier
2.	Realization of digital circuits using Multi-Valued Logic
3.	Design of Digital Circuits based on Genetic Algorithm
4.	Design and evaluation of MVL applications using CNTFET
5.	Implementation of Digital Circuits using Multiple Valued Logic
6.	Implementation of anti rigging voting system
7.	Digital Counter Design using CNTFETs

PERSONAL DETAILS:

Name	: M.Mani kumari
Father's Name	: M.Balayya
Sex	: Female
Marital status	: Married
Date of Birth	: 12th July, 1983
Contact numbers	: 9849619707
Email	: viswaravi.mani@gmail.com
Languages known	: English,Telugu and Hindi

I hereby declare that all the statements made above are correct to the best of my knowledge and belief. I also understand that any discrepancy found in the above information will render me liable for disqualification at any stage.

Place: Visakhapatnam

Date : 5/12/2019

Yours sincerely,

(M.Mani kumari)