RESUME

CH.SIRISHA,	
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Professional Summary:

- Around ten+ years of teaching experience in UG and 8+ years of teaching experience in PG.
- Proficient in teaching the subjects which are given to me. The subjects taught are:
    - Microcontrollers and its applications
    - Microprocessors and Interfacing
    - Microprocessors and Microcontrollers
    - Embedded systems
    - Embedded real time operating systems
    - DSP processors and architecture
    - Switching theory and logic designs
    - Cellular and Mobile communications
    - Hardware Software Co Design
    - Embedded C
    - Microcontrollers for Embedded Systems Design
- Registered for part time Ph.D in Andhra university.
- Excellent communication and organizational skills, Self-motivated, hard working, ability to adapt quickly to the changing environment and needs.
- Good Analytical and decision making Skills and good at time management.

- I got the certificate of appreciation on 5th September 2017, for the contribution of work during academic year 2016-17

Work Experience:

- Worked as an Assistant professor in "MLRIT, Dundigal, Hyderabad" from Dec 2008 to 5th May 2010.
- Working as an Assistant professor in "GVPCEW, Visakhapatnam" from june 21st,2010 till date.

Memberships in Professional Bodies:

Life membership of IAENG International Association of Engineers (Member ID-225381)

Professional Activities:

1. M.Tech Coordinator for the past 5 years.
2. NBA Coordinator of the Department for the past three years.
3. Spot coordinator for PG during 2017.
4. Member of Grievance Redressal Committee in the college for three years.
5. Worked as organizing member for many events in the college.

Certifications:

The following are the NPTEL certification done:

1. Embedded System Design
2. Digital Circuits, October'18 (ELITE)
3. Microprocessors and Microcontrollers, May'19 (ELITE + SILVER)

Journals Publications:

1. **Low-power, Low-Transition Test Pattern Generator in Logic BIST Schemes**, G.Naga Seeta, Ch.Sirisha, International Journal Of Scientific & Engineering Research, VOLUME 5, ISSUE 9, SEPTEMBER-2014, ISSN 2229-5518.

2. **Performance Optimization of Dynamic and Domino logic Carry Look Ahead Adder using CNTFET in 32nm technology,** A.Naga Lakshmi, Ch.Sirisha, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 5, Issue 5, Ver. I (Sep - Oct. 2015), PP 30-35 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197 www.iosrjournals.org

3. **A probably Secure ARM based Health Monitoring system through Hybrid Crytography using Embedded System,** Ch.Sirisha, N. Navya, ISSN: 2278 – 909X International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 5, Issue 9, September 2016.

4. **VLSI Implementation of low power and Resource efficient IFO Estimation with High speed Architecture,** R. Roopa Sree, Ch.Sirisha, International Journal of Applied Sciences, Engineering and Management, ISSN 2320 – 3439, Vol. 06, No. 04, July 2017, pp.23-29.

5. **Hybrid CMOS-CNFET based NP dynamic carry look ahead adder**, A. Nagalakshmi, Ch. Sirisha, Dr. D.N. Madhusudana Rao, https://arxiv.org/abs/1805.04074, Cornell university library

6. **Machine Learning in Automated Intelligent Surveillance System**, G. Sree Laxmi, CH. Sirisha, International Journal of Electrical Communication Engineering Vol. 4: Issue1 www.journalspub.com

Workshops/ FDPs participated/ organized:

1. Participated in FDP "Advanced Android Development Program" from 14th October to 12th December, 2015 organized by APSSDC at GVP(A).

2. Organizing Committee of a Three day FDP "Electromagnetics and RF Fundamentals" held on 22nd – 24th January, 2016.

3. Participated in one week FDP "Wireless Communication Technologies" from 29th August to 3rd September, 2016 organized by E & ICT academy, NIT Warangal at GVP (A) and obtained grade A in the test.

4. Organizing Committee of a Three day National workshop on "Cryptology and Cyber Security (WCCS-2018)" sponsored by CRSI, Kolkata at GVPCEW.

5. Three day National Workshop "Cryptology and Cyber Security" Organizing Committee
6. Participated in a two week FDP "Pedagogical Training on Outcome based education" from 18th to 30th Dec, 2017 organized by GVP(A).
7. Organizing Committee of a Three day FDP "Signal Processing and Communication Systems" held on 15th to 17th November, 2017.
8. Women Entrepreneurship Development Programme- NI MSME, Participated, March, 2018
9. Organizing Secretary of a three day workshop on "Custom Analog & Digital IC Design using Mentor EDA Tool", 27th -29th September,2018
10. Participated in One week national workshop on "Machine Intelligence in Smart grid & Communication" in GVP(A), 6th -10th May' 2019.

Technical skills:

- Operating Systems : UNIX ,RTOS (VxWorks, Symbian)
- Languages : C and Data Structures, C++
- ALP : 8051,8085,8086 programming
- Packages : A+ Hardware Certification.

Educational Qualifications:

Academic record at Postgraduate level:

Degree	: Master of Technology (M.Tech)
Branch	: Digital Communications Engineering
College	: KITS, Warangal.
Affiliation	: Kakatiya University
Aggregate	: 76.65%
Year of graduation	: 2007

Academic record at Undergraduate level:

Degree	: Bachelor of Engineering (B.E)
Branch	: Electronics and Communication Engineering (E.C.E).
College	: GITAM College of Engineering, Visakhapatnam.

Affiliation : Andhra University.

Aggregate : 66%

Year of graduation : 2004

➢ Academic record at School and College:

- Completed 10th standard in CBSE stream in Kendriya Vidyalaya Waltair, Visakhapatnam in the year 1998 with an overall percentage of 68%.
- Completed Intermediate in Vikas Junior college, Visakhapatnam in the year 2000 with an overall percentage of 84%.

Extra Curricular Activities:

- Managing techno Symposium (A National Level Technical Symposium, INTERFACE 2004 held at GITAM College).
- Member of Organizing Committee for "ASPCS-05"-A workshop on "Advances in Signal Processing and Communication Systems" organized by KITS, Warangal.

Technical Projects:

- At the undergraduate level, as a part of BE final year technical project and thesis, I completed a working model on **''REMOTE CONTROL BASED ELECTRICAL APPLIANCE CONTROL".**
- At the postgraduate level, as a part of the M.Tech mini project, I completed a working model on **"THE EMULATOR BENCH"**.
- As a part of M.Tech final year technical project and thesis, I completed a working model on **"END-TO-END SECURITY FOR GSM USERS"**.

Personal Profile:

Name	:	Chimata Sirisha
Fathers Name	:	CH. MalaKondaiah
Date of Birth	:	21-06-1983
Gender	:	Female
Postal Address	:	39-8-77/4, Balaji Plaza, Flat no.103, Murali Nagar, Visakhapatnam-530007
Marital Status	:	Married
Nationality	:	Indian
Languages Known	:	English, Hindi & Telugu

I vouch for the authenticity of the above-furnished information.

CHIMATA SIRISHA