CURRICULUM VITAE

DIVYA SATHI BALAGA

E – Mail ID : ds.balaga@gvpcew.ac.in Contact no : +91 9491425382

CAREER OBJECTIVE:

Looking forward for a challenging job that enhances my technical and inter personal skills which allows me to prove my talent with true professionalism and enthusiasm.

QUALIFICATIONS :

- Postgraduate in VLSI SYSTEM DESIGN (2011-2013) from SRI SIVANI COLLEGE OF ENGINEERING (S.S.C.E., JNTUK) with **74.57%** in Dec 2013.
- Graduation in Electronics and communication engineering from SARADA INSTITUTE OF SCIENCE, TECHNOLOGY AND MANAGEMENT **(S.I.S.T.A.M., JNTUH)** with **60.04%** in April 2007.
- Board of intermediate education from SRI SAI KRISHNA Jr. College with **81.40%** in 2003.
- 10^{th}: GOVERNMENT High school with **81.33%** in Mar 2001.

PUBLICATIONS :

- **Mrs. DIVYA SATHI BALAGA**, Ms. K Bhavani, "Design of High Speed and Low Power Domino Logic Circuits for Wide Fan-in gates"., IOSR JOURNAL OF VLSI AND SIGNAL PROCESSING, ISSN: 2319-4200, 6^{TH} SEPTEMBER, 2019.
- **Mrs. DIVYA SATHI BALAGA**, Mrs. G RAJYA LAKSHMI, "GLITCH DIMINISHING POWER SUPPRESSION TECHNIQUE FOR LOW POWER MULTIPLIER", in IJIRS JOURNAL, VOLUME 2, ISSUE 8, AUGUST 2013. REFERENCE NO: 08130121/1.

MOOCS:

- Awarded **ELITE,** for successfully completing the course **"SWITCHING CIRCUITS AND LOGIC DESIGN"** with a consolidated score of **60%**, a 12-week course in association with **NPTEL (MHRD, govt of India), IIT, KHARAGPUR & SWAYAM** in 2018.

- Awarded **ELITE,** for successfully completing the course **"MICROELECTRONICS: DEVICES TO CIRCUITS"** with a consolidated score of **69%**, a 12-week course in association with **NPTEL (MHRD, govt of India) IIT, ROORKEE & SWAYAM** in 2019.

WORKSHOPS :

- Participated in a five-day faculty development programme on **"OUTCOME BASED TEACHING, LEARNING AND ASSESSMENT STRATEGIES TO ENHANCE QUALITY OF ENGINEERING EDUCATION**", organized by GVPCE(A), during 12-16 November, 2019.
- Participated in a one-day seminar on "**ROLE OF IT IN THE NEW AGE BROADCASTING**", organized by GVPCEW, in collaboration with BROADCAST ENGINEERING SOCIETY (INDIA), HYDERABAD CHAPTER, on 27th July, 2019.
- Participated in a three-day national workshop on **"CRYPTOLOGY AND CYBER SECURITY (WCCS 2018)"**, sponsored by cryptology research society of india, Kolkata organized by GVPCEW, during 22-24 march, 2018.
- Attended a three-day workshop on **"CUSTOM ANALOG & DIGITAL IC DESIGN USING MENTOR EDA TOOLS"** organized by Department of ECE, GVPCEW during 27-29 September, 2018.
- Participated in a three-day faculty development programme on "**SIGNAL PROCESSING AND COMMUNICATION SYSTEMS**" held on 15th – 17th November, 2017 organized by GVPCEW.
- Participated in a two-week ISTE STTP on "**CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN**" conducted by IIT KHARAGPUR from 26th December,2016 to 4th February,2017, with a grade" GOOD".
- Attended a three-day staff development programme on "**ELECTROMAGNETICS AND RF FUNDAMENTALS**" during 22nd to 24th January ,2016, organized by dept of ECE, GVPCEW.
- Attended a two-day national workshop on "**COGNITIVE RADIO TECHNOLOGIES**" organized by Department of ECE, GVP College of engineering for women, Visakhapatnam in September 2015.

- Participated in three week "**INDUCTION TRAINING FOR FACULTY POSITION" (ITFP)** program conducted by GVPCE(A), from 8th july to 1st august 2015.
- Attended a two day national workshop on **"VLSI DESIGN MENTOR GRAPHIC TOOL**" organized by **Xilinx** using **Xilinx 14.1SE** held in MVGR, Vizianagaram in Dec 2013
- Attended one day national workshop on "**DIGITAL COMMUNICATION LABORATORY**" organized by Department of E C E, held in MVGR, Vizianagaram on July 2012.
- Participated in the medical camp organized on 27th September, 2015 in kovvada village of padmanabham mandalam, Visakhapatnam organized by ANDHRA UNIVERSITY Teacher's Sri Satya Sai Seva Association.
- Participated in the medical camp organized on 23rd October, 2016 in gottupalli village of anandapuram mandalam, Visakhapatnam organized by ANDHRA UNIVERSITY Teacher's Sri Satya Sai Seva Association.
- Participated in the medical camp organized on 21st February, 2016 in a.koduru village of k kotapadu mandalam, Visakhapatnam organized by ANDHRA UNIVERSITY Teacher's Sri Satya Sai Seva Association.

EXPERIENCE :

- Working as assistant professor in Gayatri vidya Parishad college of engineering for women, from 3rd August, 2015 to till date.

PROJECT WORK :

- **M.Tech** Project: 'Glitch diminishing power suppression technique for low power multiplier'.

  Software used: Xilinx.
- **B.Tech** Project: 'Frequency measurement by using FPGA and VHDL' coding.

  Place: BEL Hyderabad.

  Software used: Active HDL.

PERSONAL DETAILS:

Name	:	Mrs. DIVYA SATHI BALAGA
Date of birth	:	15 July, 1986.
Marital status	:	married.
Address	:	door no:7-117 New rama nagar, near svk rice & oil mill, D C C B E colony, Srikakulam, Srikakulam – 532001.

DECLARATION :

I hereby declare that the above-mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

(DIVYA SATHI BALAGA)