II B.Tech. I Semester – Regular Examinations, Nov – 2025

Subject Name:	Linear ICs & Applications [24EC11RC09]	**Max. Marks: 70 M**
Faculty Name :	P V K Chaitanya	**Branches: ECE**

SCHEME OF VALUATION

Q No	Weightage	Total Marks
1 (a)	Derive the frequency response of an op-amp and explain the concept of slew rate Frequency response of op-amp --- 4M Slew Rate --- 3M	7
1 (b)	Discuss various compensation techniques used to improve stability. Dominant Pole Compensation --- 4M Pole-Zero Compensation --- 3M	7
2 (a)	Explain the internal block diagram of 741 op-amp with neat sketch. Internal block diagram and pin diagram --- 4M Explanation --- 3M	7
2 (b)	Analyze the parameters affecting op-amp performance in linear region. Any 4 { DC Parameters --- 4M AC Parameters --- 3M	7
3 (a)	Design and analyze an op-amp based inverting and non-inverting amplifier. Inverting amplifier design and analysis --- 3.5M Non-Inverting amplifier design and analysis --- 3.5M	7
3 (b)	Explain the operation of integrator and differentiator circuits. Integrator circuit and operation --- 3.5M Differentiator circuit and operation --- 3.5M	7
4 (a)	Explain the operation of Adder and Subtractor circuits using OP-AMP. Adder circuit and operation --- 3.5M Subtractor circuit and operation --- 3.5M	7
4 (b)	Derive the expression for frequency of oscillations of an RC phase shift oscillator. Circuit Diagram --- 2M Derivation for f_o --- 5M	7
5 (a)	Explain the design of a Schmitt Trigger Circuit using OP-AMP. Circuit Diagram --- 2M Design explanation --- 5M	7

Gayatri Vidya Parishad College of Engineering for Women (Autonomous)

Madhurawada, Visakhapatnam

(Affiliated to Andhra Jniversity, Visakhapatnam)

II B.Tech. I Semester – Regular Examinations, Nov – 2025

5 (b)	**Explain the operation of a monostable multivibrator circuit.** Circuit Diagram --- 2M Explanation --- 5M	7
6 (a)	**Describe the working of active filters and derive transfer functions for LPF and HPF.** LPF Circuit and Transfer fn. derivation --- 3.5M HPF Circuit and Transfer fn. derivation --- 3.5M	7
6 (b)	**Discuss the effect of finite open loop gain on filter response.** Effect of finite open loop gain on filter response --- 7M	7
7 (a)	**Explain the working of ADC using successive approximation method.** Circuit Diagram --- 2M Explanation --- 5M	7
7 (b)	**Derive the relation between resolution and quantization error in DAC.** Resolution --- 2M Quantization error --- 2M Relation --- 3M	7
8 (a)	**Design a 4-bit binary-weighted DAC using op-amps and resistors.** Circuit Diagram --- 2M Explanation --- 5M	7
8 (b)	**Compare R–2R ladder and binary-weighted DACs in terms of accuracy and linearity.** R–2R ladder DAC --- 2M binary-weighted DAC --- 2M Comparison of accuracy and linearity --- 3M	7
9 (a)	**Describe the functional block diagram and working of 555 timer in astable mode.** Circuit Diagram --- 2M Explanation --- 5M	7
9 (b)	**Discuss applications of 555 timer as monostable multivibrator.** Any 2 applications --- 7M	7
10 (a)	**Explain the functional diagram of PLL and its applications in frequency synthesis.** Diagram of PLL --- 4M Application in Frequency Synthesis --- 3M	7
10 (b)	**Analyze VCO characteristics and lock range of PLL circuits.** VCO Characteristics --- 4M Lock range of PLL circuits --- 3M	7

Verified

(Dr. M. Mani Keemari)

P V K Chaitanya

Assistant Professor

Department of ECE