Gayatri Vidya Parishad College of Engineering for Women (Autonomous)

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(Affiliated to Andhra University, Visakhapatnam)

II B.Tech. I Semester – Regular Examinations, Nov – 2025

Subject Name: Linear ICs & Applications [24EC11RC09] **Max. Marks: 70 M**

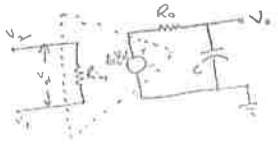
Faculty Name : P V K Chaitanya **Branches: ECE**

ANSWER KEY

Q No	Weightage	Total Marks
1 (a)	**Derive the frequency response of an op-amp and explain the concept of slew rate**	7

Frequency Response

Corner frequency
(or)
break frequency



High frequency Model of Op Amp

A_{OL} → Open loop gain

A → Open loop gain with one corner frequency

$$V_o = \frac{-jX_c}{R_o - jX_c} \cdot A_{OL} V_d$$

$$\Rightarrow \frac{V_o}{V_d} = \frac{-jX_c}{R_o - jX_c} \cdot A_{OL}$$

$$\Rightarrow A = \frac{(-jX_c)/(-jX_c)}{(R_o - jX_c)/(-jX_c)} \cdot A_{OL} = \frac{1}{1 - \frac{R_o}{jX_c}} \cdot A_{OL}$$

$$= \frac{1}{1 + j\omega R_o C} A_{OL} = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

$$\Rightarrow \boxed{A = \frac{A_{OL}}{1 + j(f/f_1)}}$$

$$\frac{1}{2\pi R_o C} = f_1$$

$$\boxed{|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}}$$

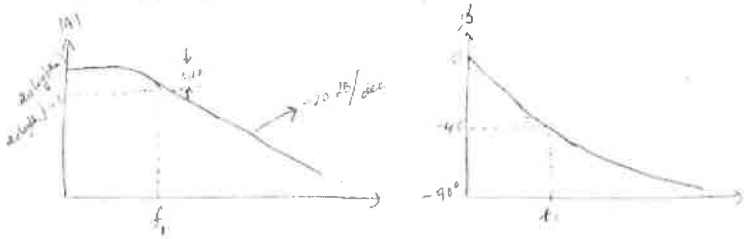
$$\boxed{\phi = -\tan^{-1}(f/f_1)}$$

if $f \ll f_1$, then $|A| = |A_{OL}|$, $\phi = 0$

if $f = f_1$, then $|A| = \frac{|A_{OL}|}{\sqrt{2}}$, $\phi = -45^\circ$

if $f \gg f_1$, then $|A|$ decreases

if $f = \infty$, then $|A| = 0$, $\phi = -90^\circ$



$$A = \frac{A_{OL}}{1 + j\left(f/f_1\right)} = \frac{A_{OL}}{1 + j\left(\omega/\omega_1\right)}$$

$$= \frac{\omega_1 A_{OL}}{\omega_1 + j\omega}$$

$$\boxed{A = \frac{A_{OL}\,\omega_1}{s + \omega_1}}$$

Practically, an opamp has a no. of stages and so, each stage produces a capacitive component

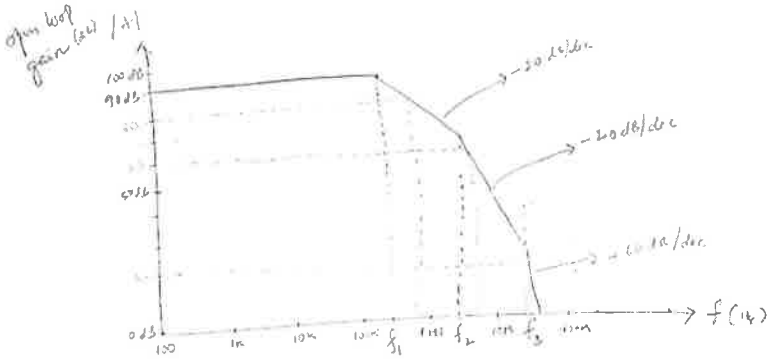
Let us consider, that there are 3 such capacitive components

then

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

$$A = \frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

$0 < \omega_1 < \omega_2 < \omega_3$



suppose $f_1 = 200\,kHz$, $f_2 = 2\,MHz$, $f_3 = 20\,MHz$

Slew Rate

→ when $V_o > 1V$

Slew rate is defined as the maximum rate of change of output voltage

$$SR = \left.\frac{dV_o}{dt}\right|_{max.}$$

$0.1V/\mu s$ to $1000V/\mu s$

$$I = C\frac{dV_c}{dt} \qquad V_c = \frac{1}{C}\int I\,dt$$

$$\Rightarrow \frac{dV_c}{dt} = \frac{I}{C}$$

$$SR = \left.\frac{dV_c}{dt}\right|_{max.} = \left.\frac{I}{C}\right|_{max.} = \frac{I_{max}}{C} = \frac{15\mu A}{30pF}$$

$= 0.5V/\mu s$

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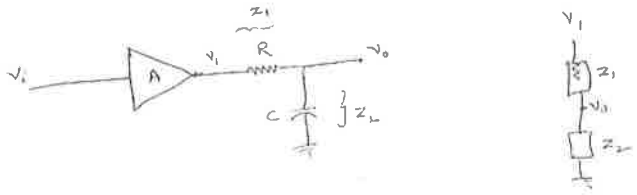
1 (b)	**Discuss various compensation techniques used to improve stability.**	7

Dominant - Pole Compensation



$$V_o = V_1 \cdot \frac{Z_2}{Z_1 + Z_2}$$

$$V_o = V_1 \cdot \frac{-j/\omega C}{R - j/\omega C}$$

$$\frac{V_o}{V_1} = \frac{-j/\omega C}{R - j/\omega C} = \frac{1}{1 - \frac{R}{-j/\omega C}} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j2\pi fRC}$$

$$\Rightarrow \boxed{\frac{V_o}{V_1} = \frac{1}{1 + jf/f_d}}$$

where $f_d = \frac{1}{2\pi RC}$

here $f_d < f_1 < f_2 < f_3$

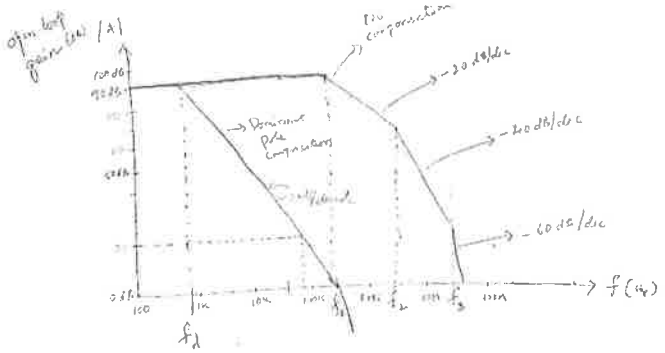
Compensated transfer function

$$A' = \frac{V_o}{V_s} = \frac{V_o}{V_1} \cdot \frac{V_1}{V_i} = A \frac{V_o}{V_i}$$

$$= \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \cdot \frac{1}{1 + jf/f_d}$$

$$\Rightarrow A' = \frac{A_{OL}}{(1 + jf/f_d)(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)}$$

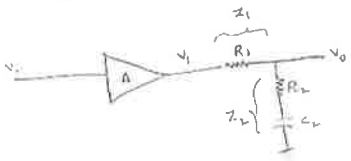
$$A' = \frac{A_{OL}\, \omega_d \omega_1 \omega_2 \omega_3}{(s + \omega_d)(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$



So, by using dominant-pole compensation, the system becomes stable for lower closed loop gains

But the BW also drastically reduces

Pole - Zero compensation



$$V_1 = V_i \frac{Z_2}{Z_1+Z_2} = V_i \times \frac{R_2 + \frac{1}{j\omega C_2}}{R_1 + R_2 + \frac{1}{j\omega C_2}}$$

$$= V_i \times \frac{R_2\left(1 + \frac{1}{j\omega R_2 C_2}\right)}{R_1 + R_2\left[1 + \frac{1}{j\omega(R_1+R_2)C_2}\right]}$$

$f_a = f_1 = \frac{1}{2\pi R_2 C_2}$

$f_b = f_0 = \frac{1}{2\pi(R_1+R_2)C_2}$

$$V_o = V_1 \times \frac{R_2}{R_1+R_2} \frac{\left(1 + j\frac{f}{f_a}\right)}{\left(1 + j\frac{f}{f_b}\right)}$$

$$\frac{V_o}{V_1} = \frac{R_2}{R_1+R_2} \frac{1+j\frac{f}{f_a}}{1+j\frac{f}{f_b}}$$

$R_2 \gg R_1$
$\therefore \frac{R_2}{R_1+R_2} \approx 1$

Transfer fn of the compensated op-amp

$$A' = \frac{V_o}{V_i} = \frac{V_o}{V_1}\frac{V_1}{V_i} = A \cdot \frac{V_o}{V_i}$$

$$= \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)} \cdot \frac{R_2}{R_1+R_2} \frac{\left(1+j\frac{f}{f_a}\right)}{\left(1+j\frac{f}{f_b}\right)}$$

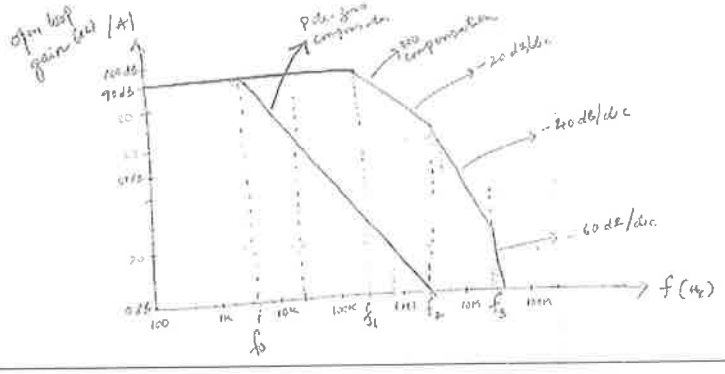
$$\Rightarrow A' = \frac{A_{OL}\left(1+j\frac{f}{f_a}\right)}{\left(1+j\frac{f}{f_b}\right)\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

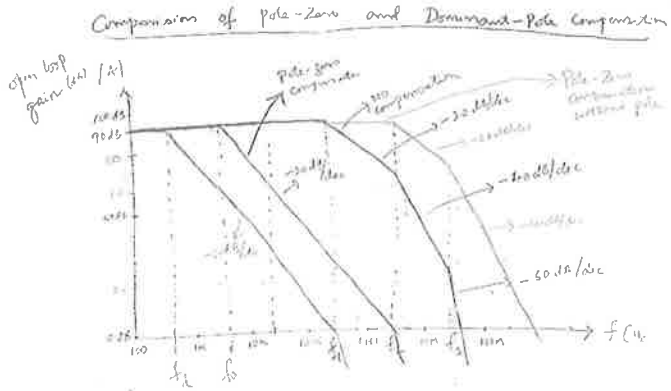
Consider, $f_a = f_1$, $f_b = f_0$ $\Big\}$ $f_0 < f_1 < f_2 < f_3$

Then $A' = \frac{A_{OL}\left(1+j\frac{f}{f_1}\right)}{\left(1+j\frac{f}{f_0}\right)\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$

$$\Rightarrow A' = \frac{A_{OL}}{\left(1+j\frac{f}{f_0}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

$$\Rightarrow A' = \frac{A_{OL}\,\omega_0\omega_2\omega_3}{(s+\omega_0)(s+\omega_2)(s+\omega_3)}$$





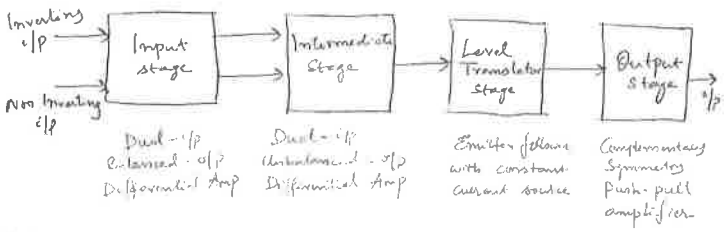
2 (a) **Explain the internal block diagram of 741 op-amp with neat sketch.** **7**

Operational Amplifier

OP-AMP

Op-amp is a direct-coupled high-gain amplifier having one (or) more differential amplifiers and usually followed by a level translator and an output stage

Block Diagram



The internal block diagram of the 741 op-amp consists of several interconnected functional stages that together provide high gain, stability, and good signal performance. At the input, a dual NPN differential amplifier stage receives the inverting (−) and non-inverting (+) signals, offering high input impedance and excellent common-mode rejection. This stage is biased by a constant current source formed using current mirrors, which ensure temperature-independent and stable operation. The differential stage feeds an intermediate high-gain voltage amplification stage, which provides most of the op-amp's open-loop gain. A level-shifting circuit is then used to adjust the DC operating point so that the output can swing around zero volts. Finally, the signal reaches a Class-AB push–pull emitter follower output stage, which provides low output impedance and sufficient load-driving capability while minimizing distortion. Overall, the 741 contains about 20 transistors and 11 resistors, and its internal design ensures high gain, good linearity, thermal stability, and reliable general-purpose amplifier performance.

2 (b) **Analyze the parameters affecting op-amp performance in linear region.** **7**

The performance of an op-amp operating in its linear region is influenced by several key electrical parameters.

Open-loop gain must be very high so that, with negative feedback, the amplifier maintains accurate, linear input–output relationships; limited gain causes gain error.

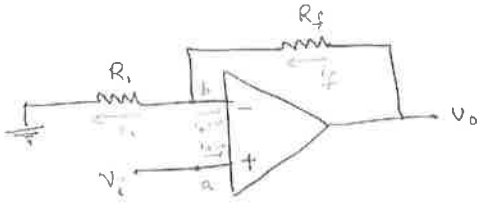
Input offset voltage introduces a small unwanted output even when both inputs are equal, affecting precision applications.

Input bias and offset currents flowing into the input terminals produce voltage drops across external resistances, creating additional offset errors.

Input impedance should be high to avoid loading the signal source,
Output impedance must be low to deliver accurate output voltage to the load.
The **gain-bandwidth product (GBW)** determines how much closed-loop gain can be achieved without losing bandwidth—higher GBW gives better high-frequency linear performance.
Slew rate limits how fast the output can change; if the input signal changes faster than the slew rate, distortion occurs even in the linear region.
Common-mode rejection ratio (CMRR) affects accuracy when the amplifier receives common-mode noise
Power-supply rejection ratio (PSRR) indicates sensitivity to supply voltage fluctuations—poor PSRR causes output variations.
Noise performance, including thermal and shot noise, affects low-level signal amplification.
Temperature stability and drift influence long-term accuracy of offset and bias values. Together, these parameters determine precision, speed, linearity, stability, and signal fidelity of the op-amp while operating within its linear region.

3 (a) Design and analyze an op-amp based inverting and non-inverting amplifier. **7**

Non-Inverting Amplifier



$V_a = V_i$

$$V_b = V_o \cdot \frac{R_1}{R_1 + R_f}$$

but $V_a = V_b$

$$\therefore V_i = V_o \frac{R_1}{R_1 + R_f}$$

$$\Rightarrow V_o = \frac{R_1 + R_f}{R_1} \cdot V_i$$

$$\Rightarrow \boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_i}$$

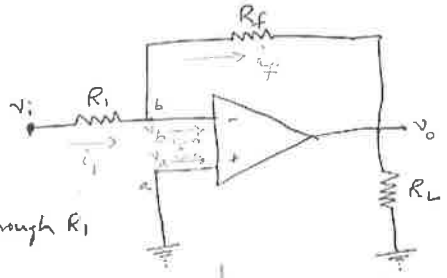
$$\boxed{A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}}$$

Inverting Amplifier

$V_a = 0$

but $V_a = V_b$

$\therefore V_b = 0$



i_1 is the current flowing through R_1

$$i_1 = \frac{V_i - V_b}{R_1}$$

$$\Rightarrow \boxed{i_1 = \frac{V_i}{R_1}} \quad \rightarrow (1)$$

i_f is the current flowing through R_f

$$\therefore i_f = \frac{V_b - V_o}{R_f}$$

$$\Rightarrow \boxed{i_f = -\frac{V_o}{R_f}} \quad \rightarrow (2)$$

Writing KCL at node a

$$i_1 = i_b + i_f$$

$$\Rightarrow i_1 = i_f$$

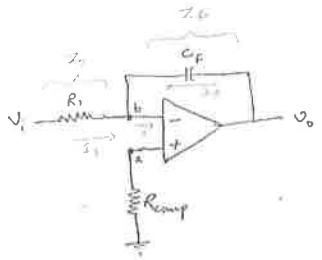
$$\frac{V_i}{R_1} = -\frac{V_o}{R_f}$$

$$\Rightarrow \boxed{V_o = -\frac{R_f}{R_1} \cdot V_i}$$

$$\Rightarrow \boxed{A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}}$$

3 (b)	**Explain the operation of integrator and differentiator circuits.**	7

Integrator



Write KCL at node 'b'

$$I_1 + I_f = 0$$

$$\frac{V_i - V_b}{R_1} + C_f \frac{d}{dt}(V_o - V_b) = 0$$

$$\Rightarrow \frac{V_i}{R_1} + C_f \frac{dV_o}{dt} = 0$$

$$\Rightarrow \frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

Integrating on both sides

$$V_o(t) = -\frac{1}{R_1 C_f} \int_0^t V_i(t)\, dt$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_1}$$

$$= -\frac{\frac{1}{sC_f}}{R_1}$$

$$\Rightarrow A = \frac{V_o(s)}{V_i(s)} = -\frac{1}{sR_1C_f}$$

In steady state

$$A = \frac{V_o}{V_i} = \frac{-1}{j\omega R_1 C_f}$$

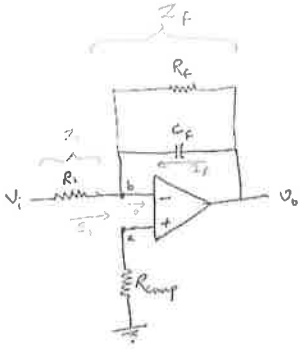
$$|A| = \left|\frac{-1}{j\omega R_1 C_f}\right|$$

$$\Rightarrow |A| = \frac{1}{\omega R_1 C_f} = \frac{1}{2\pi f R_1 C_f}$$

$$\Rightarrow |A| = \frac{1}{f/f_b} = \frac{f_b}{f} \quad \text{where } f_b = \frac{1}{2\pi R_1 C_f}$$

Practical Integrator

[Lossy Integrator]



$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_1}$$

$$= -\frac{\frac{R_f \cdot \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}}}{R_1}$$

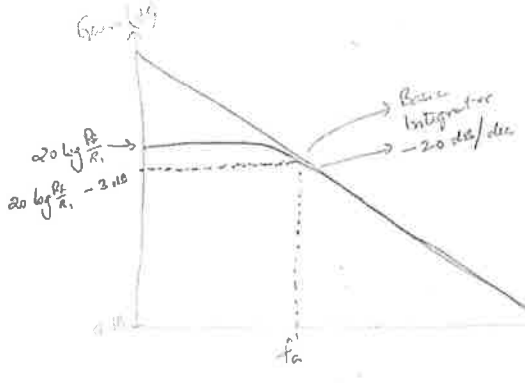
$$= -\frac{R_f}{R_1(1+sR_fC_f)}$$

$$A = \frac{V_o(s)}{V_i(s)} = -\frac{R_f/R_1}{1+sR_fC_f}$$

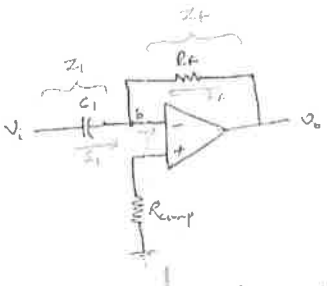
$$A = \frac{V_o}{V_i} = \frac{-R_f/R_1}{1+j\omega R_f C_f}$$

$$A = \frac{V_o}{V_i} = \frac{-R_f/R_1}{1+jf/f_a} \quad \text{where } f_a = \frac{1}{2\pi R_f C_f}$$

$$|A| = \left|\frac{-R_f/R_1}{1+jf/f_a}\right| = \frac{R_f/R_1}{\sqrt{1+(f/f_a)^2}} = \frac{R_f/R_1}{\sqrt{1+(\omega R_f C_f)^2}}$$



Differentiator



at node 'b'

$$I_1 + I_f = 0$$

$$C_1 \frac{d}{dt}(V_i - V_b) + \frac{V_o - V_b}{R_f} = 0$$

$$\Rightarrow C_1 \frac{dV_i}{dt} + \frac{V_o}{R_f} = 0$$

$$\Rightarrow V_o = -R_f C_1 \frac{dV_i}{dt}$$ ✓

Output

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_1} = \frac{-R_f}{1/sC_1}$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = -sR_f C_1$$

In steady state, $s = j\omega$

$$A = \frac{V_o}{V_i} = -j\omega R_f C_1$$

$$= -j 2\pi f R_f C_1$$

$$A = \frac{V_o}{V_i} = -j f/f_a \quad \text{where}$$

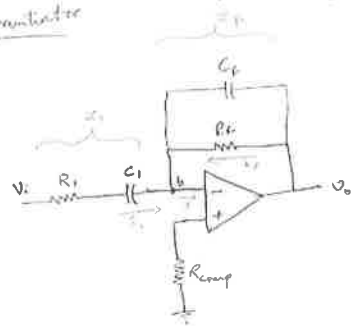
$$|A| = \left|\frac{V_o}{V_i}\right| = \left|-j f/f_a\right| = \frac{f}{f_a}$$

if $f = 0$ then $|A| = 0$

$f = f_a$ then $|A| = 1 = 0$ dB

$f = \infty$ then $|A| = \infty$

Practical Differentiator



$$\frac{V_o(s)}{V_i(s)} = \frac{-Z_f}{Z_1}$$

$$= \frac{-\frac{R_f \cdot \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}}}{R_1 + \frac{1}{sC_1}} = \frac{-\frac{R_f}{1+sR_fC_f}}{\frac{1+sR_1C_1}{sC_1}}$$

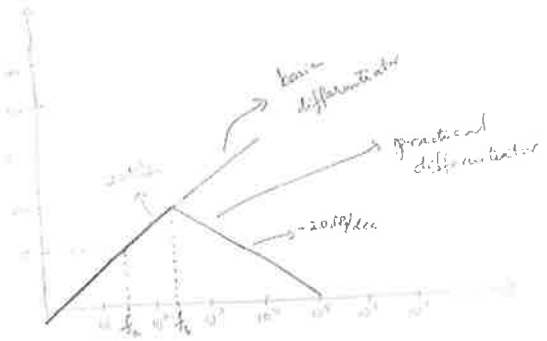
$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_fC_1}{(1+sR_fC_f)(1+sR_1C_1)}$$

let us take $R_1C_1 = R_fC_f$

then

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_fC_1}{(1+sR_1C_1)^2}$$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{jf/f_a}{(1+jf/f_b)^2}$$ where $f_a = \frac{1}{2\pi R_fC_1}$, $f_b = \frac{1}{2\pi R_1C_1}$

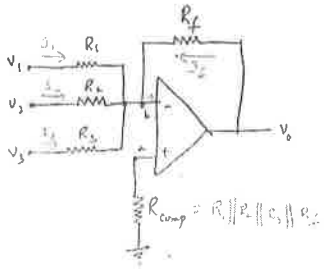


for good differentiation,

Time period of input signal, $T \geq R_fC_1$

4 (a) **Explain the operation of Adder and Subtractor circuits using OP-AMP.** **7**

Inverting Summing Amplifier



Ideally $V_a = 0V$

but $V_b = V_a$

$\therefore V_b = 0$

writing KCL at node 'b'

$I_1 + I_2 + I_3 + I_f = 0$

$$\frac{V_1 - V_b}{R_1} + \frac{V_2 - V_b}{R_2} + \frac{V_3 - V_b}{R_3} + \frac{V_o - V_b}{R_f} = 0$$

$$\Rightarrow -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) = \frac{V_o}{R_f}$$

$$\Rightarrow \boxed{V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)} \rightarrow \text{Weighted sum of the inputs}$$

if $R_f = R_1 = R_2 = R_3$

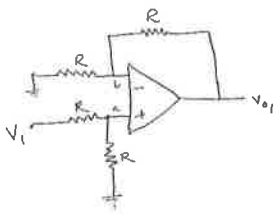
then $\boxed{V_o = -(V_1 + V_2 + V_3)} \rightarrow$ inverted sum of inputs

if $R_1 = R_2 = R_3 = 3R_f$

then $\boxed{V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right)} \rightarrow$ average of the inputs

Subtractor

firstly,
Consider input V_1
and make $V_2 = 0$



$$V_a = V_1 \cdot \frac{R}{R+R} = \frac{V_1}{2}$$

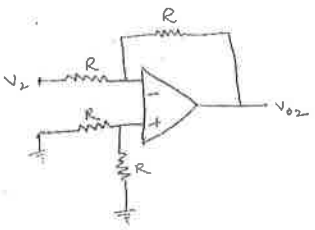
$\therefore V_b = V_a = \frac{V_1}{2}$

$$V_{o1} = \left(1 + \frac{R_f}{R_1}\right) V_b$$

$$= \left(1 + \frac{R}{R}\right) \cdot \frac{V_1}{2}$$

$$\Rightarrow \boxed{V_{o1} = V_1}$$

Similarly, consider only V_2
and $V_1 = 0V$



$$\therefore V_{o2} = -\frac{R_f}{R_1} \cdot V_{i2} = -\frac{R}{R} \cdot V_2$$

$$\Rightarrow \boxed{V_{o2} = -V_2}$$

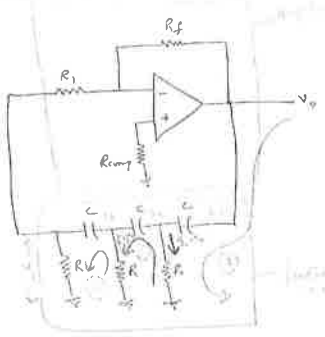
$\therefore$ Using superposition theorem

$$V_o = V_{o1} + V_{o2}$$

$$\Rightarrow \boxed{V_o = V_1 - V_2}$$

4 (b)	**Derive the expression for frequency of oscillations of an RC phase shift oscillator.**	7

RC Phase Shift Oscillator



$|A\beta| > 1$

A → Gain of actual Amp

β → Gain of feedback ckt

$V_f = I_2 R$

KVL in loop (1)

$V_0 - I_1\frac{1}{sC} - (I_1 - I_3)R = 0$

$V_0 - I_1\left(R + \frac{1}{sC}\right) + I_3 R = 0 \longrightarrow (1)$

KVL in loop (2)

$-(I_2 - I_1)R - I_2\cdot\frac{1}{sC} - (I_2 - I_3)R = 0$

$+I_1 R - I_2\left(R + \frac{1}{sC} + R\right) + I_3 R = 0$

$I_1 R - I_2\left(2R + \frac{1}{sC}\right) + I_3 R = 0 \longrightarrow (2)$

KVL in loop (3)

$-(I_3 - I_1)R - I_3\frac{1}{sC} + I_3 R = 0$

$I_2 R - I_3\left(2R + \frac{1}{sC}\right) = 0 \longrightarrow (3)$

from eqn (3)

$I_2 = I_3\left(2 + \frac{1}{sRC}\right) \longrightarrow (4)$

substituting eqn (4) in eqn (2)

$I_1 R - I_3\left(2 + \frac{1}{sRC}\right)\left(2R + \frac{1}{sC}\right) + I_3 R = 0$

$I_1 R = I_3\left(4R + \frac{2}{sC} + \frac{2R}{sRC} + \frac{1}{s^2RC^2} - R\right)$

$I_1 = I_3\left(3 + \frac{2}{sRC} + \frac{2}{sRC} + \frac{1}{s^2R^2C^2}\right)$

$I_1 = I_3\left(3 + \frac{4}{sRC} + \frac{1}{s^2R^2C^2}\right) \longrightarrow (5)$

substituting eqns (4), (5) in eqn (1)

$V_0 - I_3\left(3 + \frac{4}{sRC} + \frac{1}{s^2R^2C^2}\right)\left(R + \frac{1}{sC}\right) + I_3\left(2 + \frac{1}{sRC}\right)R = 0$

$V_0 - I_3\left(3R + \frac{3}{sC} + \frac{4R}{sRC} + \frac{4}{s^2RC^2} + \frac{R}{s^2R^2C^2} + \frac{1}{s^3R^2C^3} + 2R + \frac{R}{sRC}\right) = 0$

$I_3\left(R + \frac{3}{sC} + \frac{4}{sC} + \frac{4}{s^2RC^2} + \frac{1}{s^2RC^2} + \frac{1}{s^3R^2C^3} - \frac{1}{sC}\right) = V_0$

$I_3\left(R + \frac{6}{sC} + \frac{5}{s^2RC^2} + \frac{1}{s^3R^2C^3}\right) = V_0$

$I_3 = \frac{V_0}{R + \frac{6}{sC} + \frac{5}{s^2RC^2} + \frac{1}{s^3R^2C^3}} \longrightarrow (6)$

but $V_f = I_3 R$

$= \frac{V_0}{R + \frac{6}{sC} + \frac{5}{s^2RC^2} + \frac{1}{s^3R^2C^3}}\cdot R$

$V_f = \frac{V_0}{1 + \frac{6}{sRC} + \frac{5}{s^2R^2C^2} + \frac{1}{s^3R^3C^3}}$

$\Rightarrow V_f = \frac{V_0}{1 + \frac{6}{j\omega RC} + \frac{5}{j^2\omega^2R^2C^2} + \frac{1}{j^3\omega^3R^3C^3}}$

$= \frac{V_0}{1 + \frac{6}{j\omega RC} - \frac{5}{\omega^2R^2C^2} - \frac{1}{j\omega^3R^3C^3}}$

$V_f = \frac{V_0}{1 - \frac{5}{\omega^2R^2C^2} - j\left(\frac{6}{\omega RC} - \frac{1}{\omega^3R^3C^3}\right)}$

feedback factor

$\beta = \frac{V_f}{V_0}$

$\beta = \frac{1}{1 - \frac{5}{\omega^2R^2C^2} - j\left(\frac{6}{\omega RC} - \frac{1}{\omega^3R^3C^3}\right)}$

Consider $\alpha = \frac{1}{\omega RC}$

Then $\beta = \frac{1}{(1 - 5\alpha) - j\alpha(6 - \alpha^2)}$

$A\beta = 1 \Rightarrow \beta$ should be real

$\therefore \alpha(6 - \alpha^2) = 0$

$\Rightarrow \alpha^2 = 6$

$\Rightarrow \alpha = \sqrt{6}$

$\Rightarrow \frac{1}{\omega RC} = \sqrt{6}$

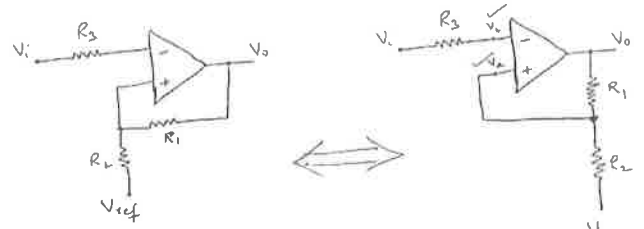
$\Rightarrow \omega = \frac{1}{\sqrt{6}RC}$

$\Rightarrow \boxed{f_0 = \frac{1}{2\pi RC\sqrt{6}}} \longrightarrow (7)$

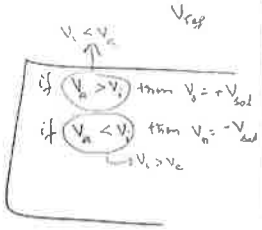
II B.Tech. I Semester – Regular Examinations, Nov – 2025

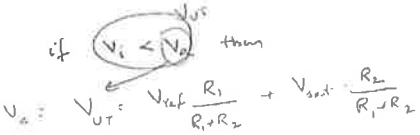
5 (a)	**Explain the design of a Schmitt Trigger Circuit using OP-AMP.**	7

Regenerative Comparator [Schmitt Trigger]

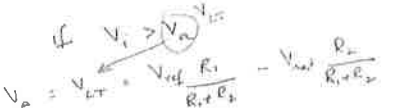


$$V_a = V_{ref}\frac{R_1}{R_1+R_2} + V_o\frac{R_2}{R_1+R_2}$$

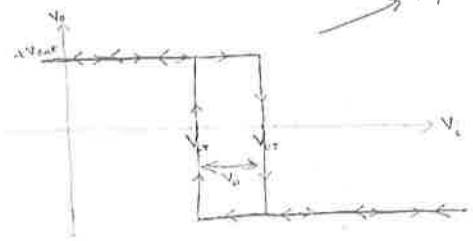




$V_{UT} > V_{LT}$



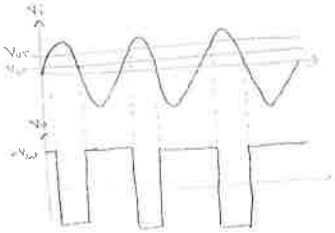
Hysteresis



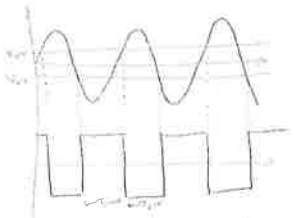
Hysteresis width $V_H = V_{UT} - V_{LT}$

$$= \left(V_{sat}\frac{R_1}{R_1+R_2} + V_{sat}\frac{R_2}{R_1+R_2}\right) - \left(V_{sat}\frac{R_1}{R_1+R_2} - V_{sat}\frac{R_2}{R_1+R_2}\right)$$

$$\Rightarrow V_H = 2V_{sat}\frac{R_2}{R_1+R_2}$$

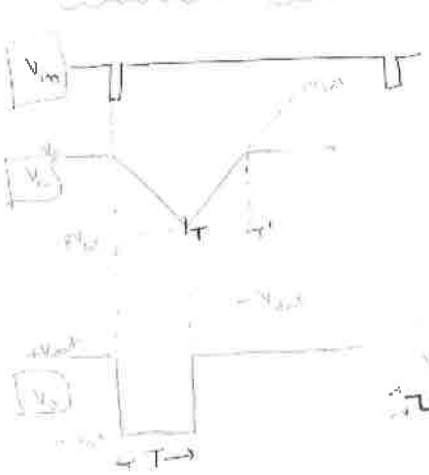


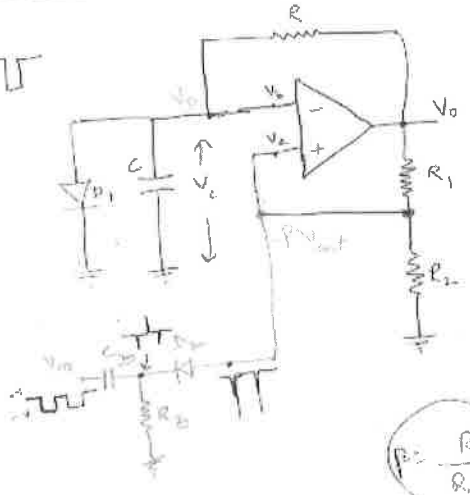
If $V_{ref} = 0V \longrightarrow V_{UT} = -V_{LT} = V_{sat}\frac{R_2}{R_1+R_2}$



5 (b)	**Explain the operation of a monostable multivibrator circuit.**	7

Monostable Multivibrator





$$\beta = \frac{R_2}{R_1+R_2}$$

$V_c = V_f + (V_i - V_f)e^{-t/RC}$

$V_i = -V_{sat}$; $V_f = V_\beta$

$\therefore V_c = -V_{sat} + (V_\beta - (-V_{sat}))e^{-t/RC}$

$V_c = -V_{sat} + (V_\beta + V_{sat})e^{-t/RC}$

at $t = T$, $V_c = -\beta V_{sat}$

$-\beta V_{sat} = -V_{sat} + (V_\beta + V_{sat})e^{-T/RC}$

$e^{-T/RC} = \frac{V_{sat}(1-\beta)}{V_\beta + V_{sat}}$

$e^{-T/RC} = \frac{1-\beta}{1+\frac{V_\beta}{V_{sat}}}$

$-\frac{T}{RC} = \ln\left(\frac{1-\beta}{1+V_\beta/V_{sat}}\right)$

$T = -RC \ln\left(\frac{1-\beta}{1+V_\beta/V_{sat}}\right)$

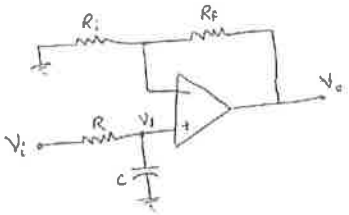
$T = RC \ln\left(\frac{1-V_\beta/V_{sat}}{1-\beta}\right)$

i) $V_{sat} \gg V_\beta$ and suppose $\beta = 0.5$

then $T = 0.693\,RC$

6 (a) **Describe the working of active filters and derive transfer functions for LPF and HPF.** **7**

First Order Low Pass Filter



$V_1(s) = V_i(s) \cdot \frac{\frac{1}{sC}}{R + \frac{1}{sC}}$

$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs+1}$

Open loop Gain of the Op Amp

$A_0 = \frac{V_o(s)}{V_1(s)} = 1 + \frac{R_F}{R_i}$

Overall Transfer function

$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)}$

$H(s) = \frac{A_0}{RCs+1}$

$s = j\omega$

$H(j\omega) = \frac{A_0}{1+j\omega RC}$; $\omega_h = \frac{1}{RC}$;

$H(j\omega) = \frac{A_0}{1+j\frac{\omega}{\omega_h}}$

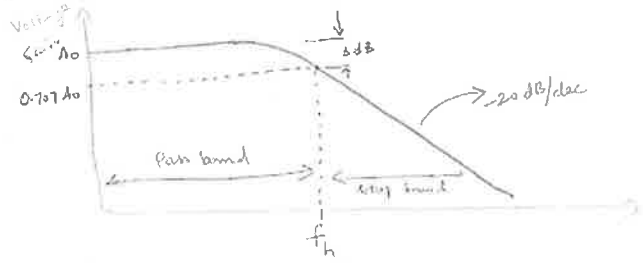
$H(j\omega) = \frac{A_0}{1+j(f/f_h)}$ $\quad |H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$

at very low freq. i.e. $f \ll f_h$ then $|H(j\omega)| \simeq A_0$

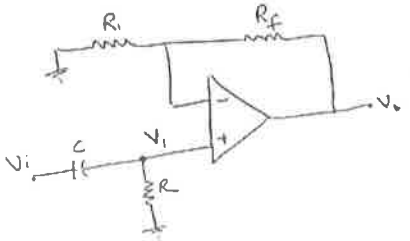
$f = f_h$ then $|H(j\omega)| = 0.707\,A_0$

if

at very high freq. i.e. $f \gg f_h$ then $|H(j\omega)| \simeq 0$



First Order High Pass Filter



$$V_1(s) = V_i(s) \times \frac{R}{R + \frac{1}{sC}}$$

$$\frac{V_1(s)}{V_i(s)} = \frac{sRC}{1+sRC}$$

Open loop gain of the Op Amp

$$A_0 = \frac{V_0(s)}{V_1(s)} = 1 + \frac{R_f}{R_1}$$

Overall Transfer function

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{V_0(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)}$$

$$= \frac{A_0 \cdot sRC}{1+sRC} = \frac{A_0}{1 + \frac{1}{sRC}}$$

$$H(j\omega) = \frac{A_0}{1 + \frac{1}{j\omega RC}}$$

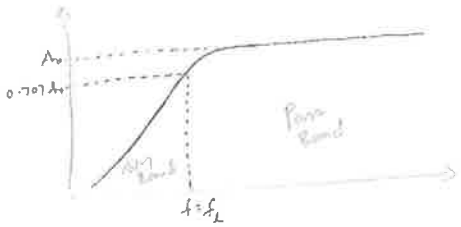
$$\Rightarrow H(j\omega) = \frac{A_0}{1 - j\left(\frac{\omega_L}{\omega}\right)}$$

$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^2}} = \frac{A_0}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}} = \frac{A_0 (f/f_L)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

if $f \ll f_L$ then $|H(j\omega)| \simeq 0$

if $f = f_L$ then $|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0$

if $f \gg f_L$ then $|H(j\omega)| \simeq A_0$



6 (b)	**Discuss the effect of finite open loop gain on filter response.**	7

1. Shift in Cutoff Frequency

In ideal analysis, the cutoff frequency f_c depends on resistor–capacitor values alone.
With finite gain, the effective circuit gain changes slightly, which shifts the actual cutoff frequency from its designed value.
Typically, Low-pass filters: cutoff frequency becomes lower than expected, High-pass filters: cutoff frequency becomes higher. This deviation increases if the closed-loop gain is high.

2. Reduction in Passband Gain

The closed-loop gain of an op-amp is ideally $A_{CL} = \frac{A_0}{1+A_0\beta} \approx \frac{1}{\beta}$
But when A_0 is finite, especially at high frequencies, Passband gain drops slightly, the filter no longer meets the exact designed gain. This is noticeable in high-gain filters or high-frequency filters.

3. Reduction in Quality Factor (Q-factor)

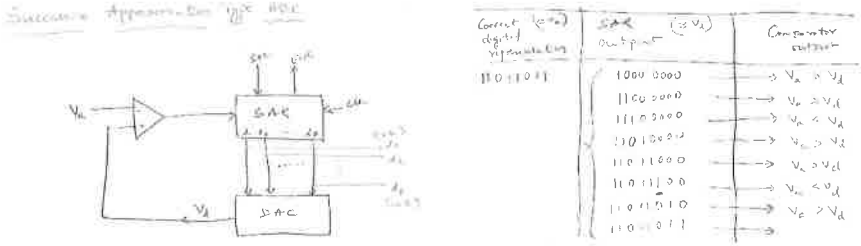
Second-order filters (Butterworth, Chebyshev, etc.) require a precise value of damping or Q.
Finite open-loop gain introduces gain error, causing, Reduced Q-factor, Less peaking near the cutoff, Broader transition band. So, the filter becomes "less selective."

4. Frequency-Dependent Distortion of Response
Since the open-loop gain falls with frequency (approx. –20 dB/decade), the effective closed-loop gain also becomes frequency-dependent. This results in: Amplitude distortion (magnitude deviates from ideal curve), Phase distortion (phase shift increases), Reduced bandwidth of accurate operation. Higher-order filters are more affected because they rely heavily on precise gain and phase.

5. Reduced Stability in High-Order Filters
Finite gain and phase shift at higher frequencies can push the filter towards instability, causing Excessive ringing, Overshoot, Undesired resonances. This is especially true for multiple feedback (MFB) and high-Q filters.

6. Increased Sensitivity to Component Tolerances
With finite A_o, small mismatches in R or C values cause larger deviations from ideal performance.
Thus, Filter responses vary more from sample to sample, Precision filter design becomes difficult

7 (a) Explain the working of ADC using successive approximation method. — 7



The SAR ADC determines the digital output **bit-by-bit** starting from the Most Significant Bit (MSB). It uses an internal DAC to generate trial voltages and a comparator to check whether the analog input is higher or lower than the generated voltage.
The working steps are:

1. Sampling
The analog input voltage V_{in} is sampled and held constant by the Sample-and-Hold circuit during the entire conversion process.

2. Set MSB = 1
The SAR sets the MSB to 1 and all other bits to 0. This digital word is applied to the DAC, which produces a trial output voltage.

3. Compare DAC Output with Input
The comparator checks:

- If V_in ≥ V_DAC → keep the MSB as 1
- If V_in < V_DAC → reset the MSB to 0

This determines the MSB of the final digital output.

4. Test the Next Bit
The SAR moves to the next bit (second MSB):

- Temporarily sets it to 1
- Keeps previously decided bits unchanged
- Sends the new digital word to DAC
- Comparator checks again and accepts or resets this bit

5. Continue for All Bits
This process continues bit-by-bit, each time refining the approximation of the input voltage.
After n such comparisons, all bits from MSB to LSB are determined.

6. Final Digital Output
After the last comparison, the SAR register contains the n-bit digital representation of the input voltage.
This completes the conversion.

7 (b) Derive the relation between resolution and quantization error in DAC. — 7

Let an n-bit DAC have a full-scale range (peak-to-peak) V_{FS} (or use reference V_{ref}). The resolution (LSB size) Δ is the smallest voltage step the DAC can produce:

$$\Delta = \text{LSB} = \frac{V_{FS}}{2^n}$$

When the analog value is represented by discrete steps of size Δ, the quantization error e (difference between the true analog value and the nearest DAC level) is bounded by half a step:

$$-\frac{\Delta}{2} \le e \le +\frac{\Delta}{2} \Rightarrow |e|_{max} = \frac{\Delta}{2}$$

So, maximum absolute quantization error = 0.5 LSB.
Therefore, quatization error = resolution /2

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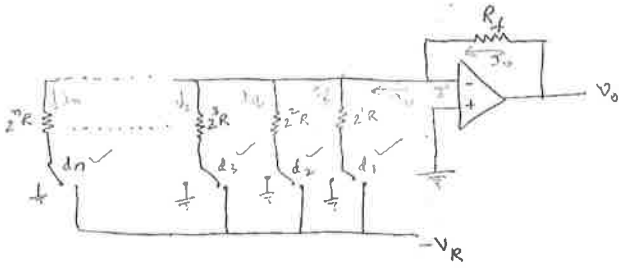
II B.Tech. I Semester – Regular Examinations, Nov – 2025

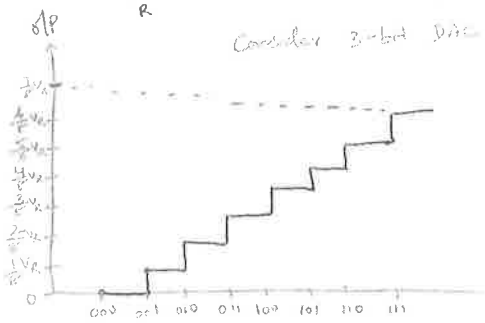
8 (a) **Design a 4-bit binary-weighted DAC using op-amps and resistors.** **7**

Weighted Resistor DAC



here $V_R = V_{FS}$

$\frac{R_f}{R} = K$



$I_o = I_1 + I_2 + I_3 + \cdots \rightarrow I_n$

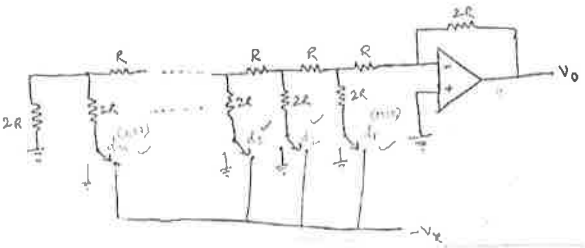
$$\frac{V_o}{R_f} = \frac{V_R}{2R}d_1 + \frac{V_R}{2^2R}d_2 + \frac{V_R}{2^3R}d_3 + \cdots + \frac{V_R}{2^nR}d_n$$

$$\frac{V_o}{R_f} = \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right)$$

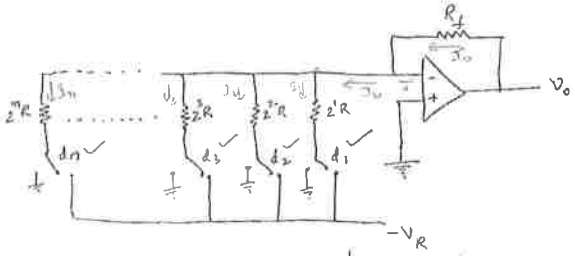
$$V_o = V_R \cdot \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right)$$

8 (b) **Compare R–2R ladder and binary-weighted DACs in terms of accuracy and linearity.** **7**

R-2R Ladder DAC



Weighted Resistor DAC



Feature	Binary-Weighted DAC	R–2R Ladder DAC
Resistor accuracy requirement	Requires resistors with values R, 2R, 4R, 8R, ... → very tight tolerance	Only two resistor values required: R and 2R, easy to match
Impact on accuracy	Difficult to fabricate accurately for large bit sizes → results in large gain errors	High accuracy because resistors are easy to match; fabrication errors are minimal
Scaling to higher resolution (8–16 bits)	Not suitable → accuracy drops significantly	Very suitable → maintains high accuracy even at high resolution
Dependence on precise resistor values	Needs large range of resistor values → mismatch causes nonlinearity, especially for MSB	All resistors of only R and 2R → excellent matching → very good linearity
INL and DNL errors	Higher INL (Integral Non-Linearity) and DNL errors	Much lower INL and DNL errors
Practical linearity performance	Poor for >8 bits	Excellent even for 12–16 bits

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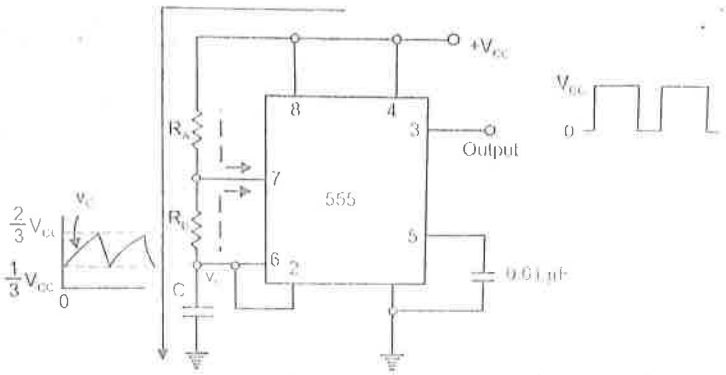
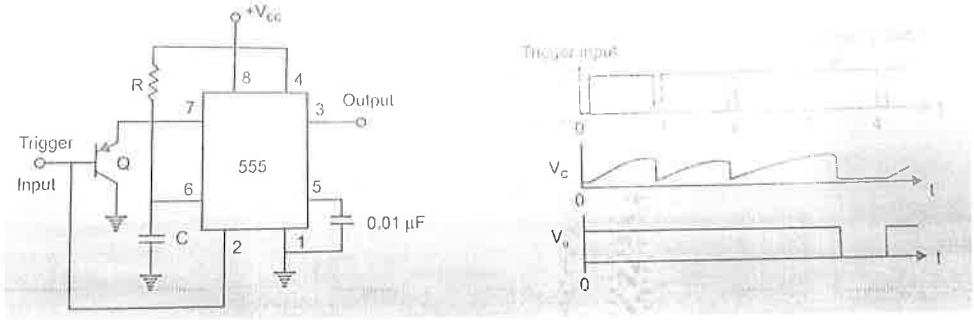
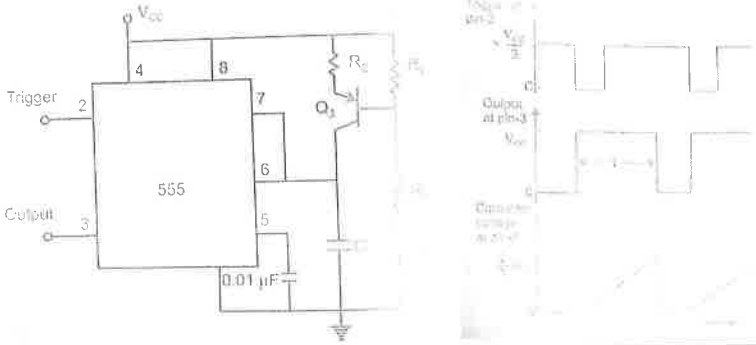
9 (a)	**Describe the functional block diagram and working of 555 timer in astable mode.** In astable mode, the 555 timer works as a continuous square-wave oscillator with no stable state. The output continuously toggles between HIGH and LOW. The external circuit uses: Two resistors: R_A and R_B, One capacitor: C These elements determine the charging and discharging time. Capacitor Charging Capacitor C charges through both resistors R_A and R_B. Charging continues until capacitor voltage reaches $\frac{2}{3}V_{CC}$. During this time, Lower comparator output = 0, Upper comparator output = 1, Flip-flop resets → Output becomes LOW, Discharge transistor turns ON → (in next stage) Capacitor Discharging When capacitor voltage reaches $\frac{2}{3}V_{CC}$, upper comparator resets the flip-flop. Now capacitor discharges only through R_B and the discharge transistor to ground. Discharging continues until capacitor voltage falls to $\frac{1}{3}V_{CC}$. When capacitor reaches $\frac{1}{3}V_{CC}$, Lower comparator sets the flip-flop, Output becomes HIGH, Discharge transistor turns OFF, Charging starts again Repeating Cycle The capacitor voltage thus repeatedly rises from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ and falls back. This causes the output to oscillate continuously → producing a square wave. Charging time (output HIGH time): $t_H = 0.693(R_A + R_B)C$ Discharging time (output LOW time): $t_L = 0.693(R_B C)$ Total Time Period: $T = t_H + t_L = 0.693(R_A + 2R_B)C$ Frequency: $f = \frac{1}{0.693(R_A+2R_B)C}$ Duty Cycle: $D = \frac{R_A+R_B}{R_A+2R_B}$ 	7
9 (b)	**Discuss applications of 555 timer as monostable multivibrator.** **Missing Pulse Detector**  **Linear Ramp Generator** 	7

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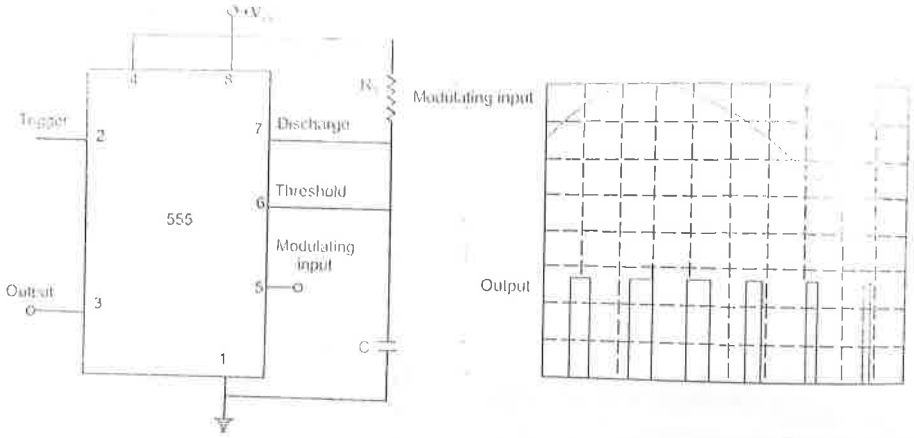
Pulse Width Modulation



10 (a)	**Explain the functional diagram of PLL and its applications in frequency synthesis.**	7

A Phase-Locked Loop consists of three main functional blocks:

1. Phase Detector (PD) compares the phase of the input signal with the phase of the output of the VCO. Produces an error signal proportional to the phase difference. Types: XOR detector, digital phase-frequency detector, mixer-type detector.

2. Low-Pass Filter (LPF) / Loop Filter Accepts the phase error signal from the phase detector, Removes high-frequency components and noise, Produces a smooth DC control voltage, Determines Loop bandwidth, Stability, Transient response,

3. Voltage-Controlled Oscillator (VCO) Generates an output frequency that depends on the input control voltage. If the control voltage increases → VCO frequency increases. If the control voltage decreases → VCO frequency decreases.

Feedback Path : The VCO output is fed back to the phase detector. In frequency synthesis, the feedback path may include a divide-by-N counter.

Working

1. Free-Running State : Initially, the VCO runs at its natural frequency without relation to the input.

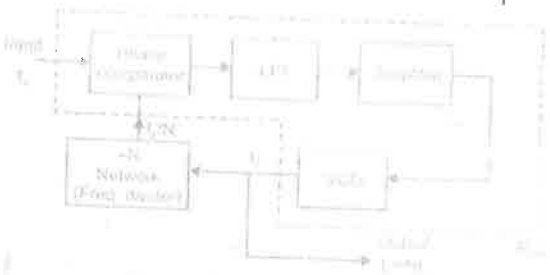
2. Capture Process : When an input signal is applied The phase detector senses a phase difference, It generates an error voltage. This adjusts the VCO frequency toward the input frequency.

3. Lock State

When the VCO frequency and phase match the input signal:The PLL is in lock condition, The error voltage becomes steady, VCO continues to follow (track) variations in input frequency.

In this state: $f_{VCO} = f_{IN}$

With a divider N in the feedback path: $f_{VCO} = N \cdot f_{IN}$



This principle is used for frequency synthesis.

Integer-N Frequency Synthesis

A divide-by-N counter is placed in the feedback loop.

VCO frequency is multiplied by integer N.

$$f_{out} = N \cdot f_{ref}$$

Used in: Radio transmitters, Digital clocks, Communication systems

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10 (b)	**Analyze VCO characteristics and lock range of PLL circuits.**	7

Derivation of Lock-in Range

$V_e = K_\phi \left(\phi - \frac{\pi}{2}\right)$

$V_c = A V_e$

$\therefore V_c = A K_\phi \left(\phi - \frac{\pi}{2}\right) \longrightarrow (1)$

$f = f_0 + K_V V_c$

if the PLL is locked, i.e. $f = f_s$

$\therefore f_s = f_0 + K_V V_c$

$\Rightarrow V_c = \frac{f_s - f_0}{K_V} \longrightarrow (2)$

from (1) & (2)

$A K_\phi \left(\phi - \frac{\pi}{2}\right) = \frac{f_s - f_0}{K_V}$

$\Rightarrow \boxed{\phi = \frac{\pi}{2} + \frac{(f_s - f_0)}{K_V K_\phi A}}$

$V_{e(max)} = \pm K_\phi \frac{\pi}{2}$

$\therefore V_{c(max)} = \pm A K_\phi \frac{\pi}{2}$

$(f - f_0)_{max} = K_V V_{c(max)}$

$= A K_V K_\phi \frac{\pi}{2}$

PLL will remain locked in th

$f_s = f_0 \pm (f - f_0)_{max}$

$f_s = f_0 \pm A K_V K_\phi \frac{\pi}{2}$

$= f_0 \pm \Delta f_L$

where $2\Delta f_L$ is lock-in range

$\Delta f_L = \pm A K_V K_\phi \frac{\pi}{2}$

$2\Delta f_L = \pm A K_V K_\phi \pi$

$\Delta f_L = \pm 1.4 \times \frac{8 f_0}{V} \times \frac{1.4}{\pi} \times \frac{\pi}{2}$

$\Rightarrow \boxed{\Delta f_L = \pm \frac{7.8 f_0}{V}}$

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