Subject Code: 24EC11RC09 **R-24** **Reg No:** | | | | | | | | | | | | |

GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING FOR WOMEN

(Autonomous)

(Affiliated to Andhra University, Visakhapatnam)

II B.Tech. - I Semester Regular Examinations, Nov – 2025

Linear ICs & Applications

1. All questions carry equal marks
2. Must answer all parts of the question at one place

Time: 3Hrs. **Max Marks: 70**

UNIT-I

1. a. Derive the frequency response of an op-amp and explain the concept of slew rate (7M)
   b. Discuss various compensation techniques used to improve stability. (7M)

OR

2. a. Explain the internal block diagram of 741 op-amp with neat sketch. (7M)
   b. Analyze the parameters affecting op-amp performance in linear region. (7M)

UNIT-II

3. a. Design and analyze an op-amp based inverting and non-inverting amplifier (7M)
   b. Explain the operation of integrator and differentiator circuits. (7M)

OR

4. a. Explain the operation of Adder and Subtractor circuits using OP-AMP. (7M)
   b. Derive the expression for frequency of oscillations of an RC phase shift oscillator. (7M)

UNIT-III

5. a. Explain the design of a Schmitt Trigger Circuit using OP-AMP. (7M)
   b. Explain the operation of a monostable multivibrator circuit. (7M)

OR

6. a. Describe the working of active filters and derive transfer functions for LPF and HPF. (7M)
   b. Discuss the effect of finite open loop gain on filter response. (7M)

UNIT-IV

7. a. Explain the working of ADC using successive approximation method. (7M)
   b. Derive the relation between resolution and quantization error in DAC. (7M)

OR

8. a. Design a 4-bit binary-weighted DAC using op-amps and resistors. (7M)
   b. Compare R–2R ladder and binary-weighted DACs in terms of accuracy and linearity. (7M)

UNIT-V

9. a. Describe the functional block diagram and working of 555 timer in astable mode. (7M)
   b. Discuss applications of 555 timer as monostable multivibrator. (7M)

OR

10. a. Explain the functional diagram of PLL and its applications in frequency synthesis. (7M)
    b. Analyze VCO characteristics and lock range of PLL circuits. (7M)