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**LECTURE SCHEDULE**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

# Branch & Section : IV B.Tech ,II Sem &ECE Regulation : R13

**Subject :** L**ow Power VLSI Design**  **Academic Year : 2017 -2018**

**Name of the Faculty :** Mrs.B.Lakshmi

**Course Objectives**

• The student will be able to understand the Fundamentals of Low Power VLSI Design.

• In this course, students can study low-Power Design Approaches, Power estimation and

analysis.

• Another main object of this course is to motivate the graduate students to study and to

analyze the Low-Voltage Low-Power Adders, Multipliers.

• The concepts of Low-Voltage Low-Power Memories and Future Trend and Development

of DRAM.

**Course Outcomes**

• Understand the concepts of Low-Power Design Approaches.

• Design and analysis of Low-Voltage Low-Power Circuits.

• Extend the Low Power Design to Different Applications.

• Understand of Low-Voltage Low-Power Memories and Basics of

DRAM.

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| Unit | Topic | | No. of Classes |
| 1. **FUNDAMENTALS OF LOW POWER VLSI DESIGN** | Need for Low Power Circuit Design | | 1 |
| **Sources of Power Dissipation** – Switching Power Dissipation | | 2 |
| Short Circuit Power Dissipation | | 1 |
| Leakage Power Dissipation, | | 1 |
| Glitching Power Dissipation | | 1 |
| **Short Channel Effects** –Drain Induced Barrier Lowering and  Punch Through | | 2 |
| Surface Scattering, Velocity Saturation | | 1 |
| Impact Ionization and  Hot Electron Effect | | 1 |
| **II. LOW-POWER**  **DESIGN**  **APPROACHES** | **Low-Power Design through Voltage Scaling** :VTCMOS circuits | | 2 |
| MTCMOS circuits | | 2 |
| Architectural Level Approach –Pipelining and Parallel  Processing Approaches | | 3 |
| **Switched Capacitance Minimization Approaches:** System Level Measures | | 2 |
| Circuit Level Measures | | 1 |
| Mask level Measures. | | 1 |
| **III POWER**  **ESTIMATION AND**  **ANALYSIS** | SPICE circuit simulators | | 2 |
| Gate level logic simulation | | 2 |
| Capacitive power estimation | | 2 |
| Static state power and gate level  capacitance estimation. | | 2 |
| 1. **LOW-VOLTAGE LOW-POWER ADDERS** | Introduction, Standard Adder Cells | 2 | |
| **CMOS Adder’s Architectures** – Ripple Carry Adders and its properties. | 1 | |
| Carry Look-Ahead Adders | 1 | |
| Carry Select Adders | 1 | |
| Carry Save Adders | 2 | |
| **Low-Voltage Low-Power Design Techniques** –Trends of Technology and Power Supply Voltage | 1 | |
| Low-Voltage Low-Power Logic Styles. | 2 | |
| 1. **LOW-VOLTAGE LOW-POWER MULTIPLIERS** | Introduction, Overview of  Multiplication | 1 | |
| **Types of Multiplier Architectures**: Braun Multiplier, | 3 | |
| Baugh-Wooley Multiplier |
| Booth Multiplier | 2 | |
| Introduction to Wallace Tree  Multiplier. | 3 | |
| 1. **LOW-VOLTAGE LOW-POWER MEMORIES** | Basics of ROM | 2 | |
| Low-Power ROM Technology | 1 | |
| Future Trend and Development of ROMs | 1 | |
| Basics of SRAM | 2 | |
| Memory Cell, Precharge and Equalization Circuit | 2 | |
| Low-Power SRAM Technologies | 1 | |
| Basics of DRAM, Self-Refresh Circuit | 2 | |
| Future Trend and Development of DRAM | 1 | |

**Total No. of Periods**: 10+11+8+10+9+12= 60

**TEXT BOOKS:**

1. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo,Kaushik Roy, TMH

Professional Engineering.

**REFERENCES:**

1. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C.Prasad, John Wiley &

Sons, 2000.

2. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.