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II YEAR B.TECH II SEMESTER-CSE – CO QUIZ TEST

1) The small extremely fast, RAM's are called as _____
a) Cache b) Registers c) Accumulators d) Stacks (a)

2) The ALU makes use of _____ to store the intermediate results.
a) Accumulator b) Registers c) memory d) Stack (b)

3) The control unit controls other units by generating ____ signals
a) Control b) Timing c) Transfer s d) Command (b)

4) The Input devices can send information to the processor. (a)
a) When the SIN status flag is set b) When the data arrives regardless of the SIN flag
c) Neither of the cases d) Either of the cases

5) ____ bus structure is usually used to connect I/O devices.
a) Single bus b) Multiple bus c) Star bus d) Rambus (a)

6) The I/O interface required to connect the I/O device to the bus consists of _____
a) Address decoder and registers b) Control circuits
c) Address decoder, registers and Control circuits d) Only Control circuits (c)

7) To reduce the memory access time we generally make use of _____ (d)
a) Stack b) Higher capacity RAM's c) SDRAM's d) Cache's

8) ____ is generally used to increase the apparent size of physical memory. (b)
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks

9) MFC stands for _____ (b)
a) Memory Format Caches b) Memory Function Complete
c) Memory Find Command d) Mass Format Command

10) The time delay between two successive initiations of memory operation _____ (c)
a) Memory access time b) Memory search time c) Memory cycle time d) Instruction delay

11) In case of, Zero-address instruction method the operands are stored in _____ (c)
a) Registers b) Accumulators c) Push down stack d) Cache

12) The addressing mode which makes use of in-direction pointers is _____ (a)
a) Indirect addressing mode b) Index addressing mode
c) Relative addressing mode d) Offset addressing mode

13) The addressing mode/s, which uses the PC instead of a general purpose register is ___
a) Indexed with offset b) Relative c) direct d) both Indexed with offset and direct (b)

14) When we use auto increment or auto decrements, which of the following is/are true? (b/d)
a) In both, the address is used to retrieve the operand and then the address gets altered
b) In auto increment the operand is retrieved first and then the address altered
c) In auto decrement the operand is retrieved first and then the address altered
d) Both of them can be used on general purpose registers as well as memory locations

15) The addressing mode, where you directly specify the operand value is _____
a) Immediate b) Direct c)register d) Relative (a)

16) The effective address of the following instruction is, MUL 5(R1,R2).
a) 5+R1+R2 b) 5+(R1*R2) c) 5+[R1]+[R2]. d) 5*([R1]+[R2]) (c)

17) _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
a) Relative b) Indirect c) Index with Offset d) Immediate (a)

18) ____ converts the programs written in assembly language into machine instructions.
a) Machine compiler b) Interpreter c) Assembler d) Converter (c)

19) The instructions like MOV or ADD are called as _____
a) OP-Code b) Operators c) Commands d) None of the mentioned (a)

20) Instructions which wont appear in the object program are called as _____ (d)
a) Redundant instructions b) Exceptions c) Comments d) Assembler Directives

21) The assembler directive EQU, when used in the instruction : Sum EQU 200 does _____ (b)
a) Finds the first occurrence of Sum and assigns value 200 to it b) Replaces every occurrence of Sum with 200
c) Re-assigns the address of Sum by adding 200 to its original address
d) Assigns 200 bytes of memory starting the location of Sum

22) The purpose of the ORIGIN directive is _____ (a)
a) To indicate the starting position in memory, where the program block is to be stored
b) To indicate the starting of the computation code
c) To indicate the purpose of the code d) To list the locations of all the registers used

23) The last statement of the source program should be _____ (d)
a) Stop b) Return c) OP d) End

24) The assembler stores all the names and their corresponding values in _____ (b)
a) Special purpose Register b) Symbol Table c) Stack d) None of the mentioned

25) The assembler stores the object code in _____ (d)
a) Main memory b) Cache c) RAM d) Magnetic disk

26) The utility program used to bring the object code into memory for execution is _____ (a)
a) Loader b) Fetcher c) Extractor d) Linker

27) To overcome the problems of the assembler in dealing with branching code we use _____
a) Interpreter b) Debugger c) Op-Assembler d) Two-pass assembler (d)

28) The return address of the Sub-routine is pointed to by _____
a) IR b) PC c) MAR d) Special memory registers (b)

29) The order in which the return addresses are generated and used is _____
a) LIFO b) FIFO c) Random d) Highest priority (a)

30) The appropriate return addresses is obtained by the help of ____ in case of nested routines.
a) MAR b) MDR c) Buffers d) Stack-pointers (d)

31) The most Flexible way of logging the return addresses of the sub routines is by using _____
a) Registers b) Stacks c) Memory locations d) None of the mentioned (b)

32) RTN stands for _____ (a)
a) Register Transfer Notation b) Register Transmission Notation
c) Regular Transmission Notation d) Regular Transfer Notation

33) The two phases of executing an instruction are _____ (b)
a) Instruction decoding and storage b) Instruction fetch and instruction execution
c) Instruction execution and storage d) Instruction fetch and Instruction processing

34) The Instruction fetch phase ends with _____ (d)
a) Placing the data from the address in MAR into MDR b) Placing the address of the data into MAR
c) Completing the execution of the data and placing its storage address into MAR
d) Decoding the data in MDR and placing it in IR

35) When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____
a) Branch target b) Loop target c) Forward target d) Jump instruction (a)

36) The condition flag Z is set to 1 to indicate _____ (c)
a) The operation has resulted in an error b) The operation requires an interrupt call
c) The result is zero d)The result is not zero

37) The decoded instruction is stored in _____ (a)
a) IR b) PC c) Registers d) MDR

38) During the execution of a program which gets initialized first ? (c)
a) MDR b) IR c) PC d) MAR

39) Which of the register/s of the processor is/are connected to Memory Bus ? (b)
a) PC b) MAR c) IR d) Both PC and MAR

40) ISP stands for _____ (a)
a) Instruction Set Processor b) Information Standard Processing
c) Interchange Standard Protocol d) Interrupt Service Procedure

41) The internal Components of the processor are connected by _____ (b)
a) Processor intra-connectivity circuitry b) Processor bus c) Memory bus d) Rambus

42) The registers,ALU and the interconnection between them are collectively called as ___ (d)
a) process route b) information trail c) information path d) data path

43) The main virtue for using single Bus structure is _____ (c)
a) Fast data transfers b) Cost effective connectivity and speed
c) Cost effective connectivity and ease of attaching peripheral devices d) None of the mentioned

44) _____ are used to over come the difference in data transfer speeds of various devices. (b)
a) Speed enhancing circuitory b) Bridge circuits c) Multiple Buses d) Buffer registers

45) ANSI stands for _____ (a)
a) American National Standards Institute b) American National Standard Interface
c) American Network Standard Interfacing d) American Network Security Interrupt

46) During the execution of the instructions, a copy of the instructions is placed in the _____ (b)
a) Register b) ROM c) Stack d) Cache

47) Two processors A and B have clock frequencies of 700 MHz and 900 MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster ? (a)
a) A b) B C) Both take the same time d) Insuffient information

48) A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
a) Super-scaling b) Pipe-lining c) Parallel Computation d) None (b)

49) The clock rate of the processor can be improved by _____ (d)
a) Improving the IC technology of the logic circuits b) Reducing the amount of processing done in one step
c) By using overclocking method d) All of the mentioned

50) The ultimate goal of a compiler is to _____ (a)
a) Reduce the clock cycles for a programming task b) Reduce the size of the object code
c) Be versatile d) Be able to detect even the smallest of errors

51) SPEC stands for _____ (c)
a) Standard Performance Evaluation Code b) System Processing Enhancing Code
c) System Performance Evaluation Corporation d) Standard Processing Enhancement Corporation

52) CISC stands for _____ (c)
a) Complete Instruction Sequential Compilation b) Computer Integrated Sequential Compiler
c) Complex Instruction Set Computer d) Complex Instruction Sequential Compilation

53) Which method/s of representation of numbers occupies large amount of memory than others ? (a)
a) Sign-magnitude b) 1's compliment c) 2's compliment d) 1's & 2's compliment

54) Which representation is most efficient to perform arithmetic operations on the numbers ? (c)
a) Sign-magnitude b) 1's compliment c) 2'S compliment d) None of the mentioned

55) The processor keeps track of the results of its operations using a flags called _____ (a)
a) Conditional code flags b) Test output flags c) Type flags d) None of the mentioned

56) The register used to store the flags is called as _____ (b)
a) Flag register b) Status register c) Test register d) Log register

57) In a normal n-bit adder, to find out if an overflow as occured we make use of _____ (d)
a) AND gate b) NAND gate c) NOR gate d) XOR gate

58) The smallest entity of memory is called as _____ (a)
a) Cell b) Block c) Byte d) Unit

59) If a system is 32 bit machine , then the length of each word will be _____ (a)
a) 4 bytes b) 8 bytes c) 16 bytes d) 12 bytes

60) The type of memory assignment used in Intel processors is _____ (a)
a) Little Endian b) Big Endian c) Medium Endian d) None of the mentioned

61) During transfer of data between the processor and memory we use _____ (d)
a) Cache b) TLB C) Buffers d) Registers