B.Tech-II-CO-Unit 1- Tutorials1

Ref. "Computer Organization," by Carl Hamacher, Zvonko Vranesic and Safwat Zaky. Fifth Edition McGraw-Hill, 2002.(chapter1-problems-pp22-23)

1) List the steps needed to execute the following machine instructions:

i) Add LOCA , RO (stored in memory location INSTR 1)

ii) Add R1 , R2 , R3 (stored in memory location INSTR 2)

terms of transfers between the components PC, IR, MAR, MDR,GPRs using simple control commands.

2) (a)Give a short sequence of machine instructions for the task:

"Add the contents of memory location A to those of location B, and place the answer in location C."

Instructions i) Load LOC , R_i and ii) Store Ri , LOC

are the only instructions available to transfer data between the memory and general-purpose Register R_i .

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2 (b) Suppose that Move and Add instructions are available with the format Move/Add Location l , Location 2 These instructions move or add a copy of the operand at the first location to the second location, over writing the original operand at the second location. Location i can be in either the memory or the processor register set. Is it possible to use fewer instructions to accomplish the task in question 2 ?
If yes, give the sequence.

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3 (a) Pipelining in the RISC is more effective than in the CISC machine. Specifically, the effective value of 5 in the 7* expression for the RISC machine is 1.2, but it is only 1.5 for the CISC . Both machines have the same clock rate ,R. What is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the *N value for the CISC machine* if time for execution on the CISC machine is to be no longer than that on the RISC machine?

3 (b) Repaet (a) by considering the clock rate of RISC is 15% higher than that of CISC.

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4 (a) Section 1.5 discusses how the input and output steps Of a collection of programs such as the one shown in Figure 1.4 could be overlapped to reduce the total time needed to Execute them. Let each of the six OS routine execution intervals be 1 unit of time, with each disk operation requiring 3 units, printing requiring 3 units, and each program execution Interval requiring 2 units of time. Compute the ratio of Best overlapped time to non voverlapped time for along sequence of programs. Ignore start-up and ending transients.

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(b) program computation can be overlaped with either input or output operations or both.
Ignoring the relatively short time needed for OS routines, what is the ratio of best overlapped time to non overlap time for completing the execution of a collection of programs, where each program has about equal balance among input, compute, and output activities?

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5 (a) Program execution time, T, as defined in Section 1.6.2, is to be examined for a certain high level language program. The program can be run on a RISC or a CISC computer. Both computers use pipelined instruction execution, but pipelining in the RISC machine is more effective than in the CISC machine. Specifically, the effective value of 5 in the 7* expression for the RISC machine is 1.2, but it is only 1.5 for the CISC machine. Both machines have the same clock rate, R. What is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as A percentage of the N value for the RISC machine, if time for execution on the CISC machine is to be no longer than that on the RISC machine?

(b) Repeat Part a if the clock rate, R, for the RISC machine is 15 percent higher than that for the CISC machine.

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6 (a). Suppose that execution time for a program is directly proportional to instruction access time and that access to an instruction in the cache is 20 times faster than access to an instruction in the main memory. Assume that a requested instruction is found in the cache with probability 0.96, and also assume that if an instruction is not found in the cache, it must first be fetched from the main memory to the cache and then fetched from the cache to be executed.
Compute the ratio of program execution time without the cache to program execution time with the cache. (This ratio is usually defined as the speedup factor resulting from the presence of the cache)
6 (b) Repeat part a for a doubled cache size. Assume that he probability of not finding a requested instruction there is a cut in half.

B.Tech II-CO-Unit1-Solutions -For the Tutorials1

Ref.Solution manula of "Computer Organization," by Carl Hamacher, Zvonko Vranesic and Safwat Zaky. Fifth Edition McGraw-Hill, 2002 (pps 1-3).

1) Add LOCA , RO (stored in memory location INSTR 1)

I. Initially the address of INSTR is stored in PC.
II. Transfer the contents of register PC to register MAR.
III. Issue a Read command to memory, and then wait until it has transferred the requested word into register MDR .
IV. Transfer the instruction from MDR into IR and decode it.
V. Transfer the address LOCA from IR to MAR .
VI. Issue a Read command and wait until MDR is loaded .
VII. Transfer contents of MDR to the ALU.
VIII. Transfer contents of R0 to the ALU.
IX. Perform addition of the two operands in the ALU and transfer result into R0.
X. Transfer contents of PC to ALU .
XI. Add 1 to operand in ALU and transfer incremented address to PC

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ii) Add R1 , R2 , R3 (stored in memory location INSTR 2)

1) The First four steps are the same as in Problem 1.1
2) Transfer contents of R1 and R2 to the ALU
3) Perform addition of two operands in the ALU
4) transfer the result into R3
5) Last two steps are the same as in Problem 1.1

2. (a)

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Move  B,C
Add   A,C
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2(b)

```
Load  A,R0
Load B,R1
Add R0,R1
Store R1,C
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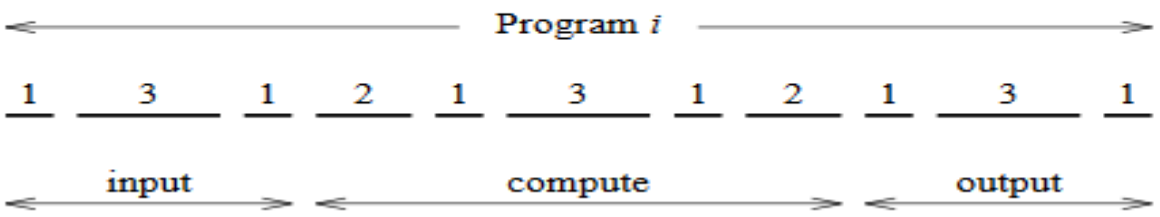
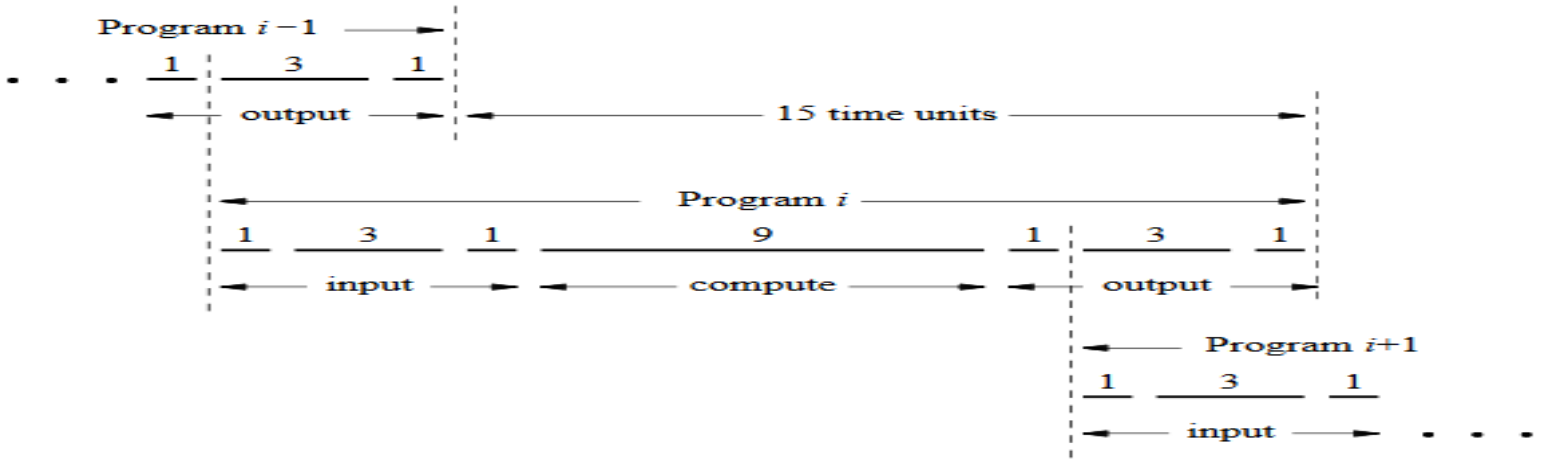
1.4. (*a*) Non-overlapped time for Program *i* is 19 time units composed as:



Overlapped time is composed as:



Time between successive program completions in the overlapped case is 15 time units, while in the non-overlapped case it is 19 time units.

Therefore, the ratio is 15/19.

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(*b*) In the discussion in Section 1.5, the overlap was only between input and output of two successive tasks. If it is possible to do output from job $i-1$, compute for job i, and input to job $i+1$ at the same time, involving all three units of printer, processor, and disk continuously, then potentially the ratio could be reduced toward 1/3. The OS routines needed to coordinate multiple unit activity cannot be fully overlapped with other activity because they use the processor. Therefore, the ratio cannot actually be reduced to 1/3.

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1.5. (a) Let $T_R = (N_R \times S_R) / R_R$ and $T_C = (N_C \times S_C) / R_C$ be execution times
on the RISC and CISC processors, respectively.
Equating execution times and clock rates, we have

$1{:}2\ N_R = 1{:}5\ N_C$

Then

$N_C / N_R = 1{:}2 / 1{:}5 = 0{:}8$

Therefore, the largest allowable value for N_C is 80% of N_R.

1.5 (b) In this case

$1.2\ N_R / 1.15 = 1.5\ N_C / 1.00$

Then

$N_C / N_R = 1.2 / (1.15 \times 1.5) = 0.696$

Therefore, the largest allowable value for N_C is 69.6% of N_R.

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6(a) Let cache access time be 1 and main memory access time be 20. Every instruction that is executed must be fetched from the cache, and an additional fetch from the main memory must be performed for 4% of these cache accesses.
Therefore,
Speedup factor = (1.0 X 20) / [(1.0 X 1) + (0.04 X 20)] = 11:1
(b) Speedup factor = (1.0 X 20) / (1.0 X 1) + (0.02 X 20) = 16:7