UNIT Wise - Previous years question papers of JNTUK University, Kakinada

Subject : Computer Architecture & Organization

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Branch : ECE

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COURSE INSTRUCTOR : Prof. Dr. E. V. Prasad

UNIT- 1: Basic Structure of Computers

1. Distinguish among computer organization and computer architecture? (4M, Nov'17)

2. Describe about memory unit? (4M, Nov'17)

3. Describe about Arithmetic Logic Unit? (4M, Nov'17)

4. Describe about control unit? (4M, Nov'17)

4. Define (r -1)'s complement and r's complement? (8M, Nov'17)

6. Give an overview of the basic functional units and bus structures of a computer? (8M, Nov'17)

14. Give an overview of the performance measurement of computers. (8M, Nov'17)

15. Write various ways to improve the clock rate? (2M, Apr'18)

16. What are the functional units of a computer system? Explain the way of handling information by each of them? (7M, Apr'18)

17. Discuss the generations of computers based on the development technologies used to fabricate the processors, memories and I/O units. (7M, Apr'18)

18. What is optimizing compiler? (2M, Apr'18)

19. Write about various general purpose registers involved in the typical computer system. (7M, Apr'18)

20. "System software is responsible for coordination of all activities in a computing system"- Justify this statement with the functionalities of it. (7M, Apr'18)

21. Write a short note on bus structures used in computer system. (2M, Apr'18)

22. Explain the importance of instruction set in measuring the performance of a computer system. (7M, Apr'18)

23. Discuss various computer types with their applications in real world environment.

(7M,Apr’18)

24. 12. What do you mean by multiprogramming? (3M, Nov’17)

25. 2. Give the major characteristics of RISC and CISC architectures. (8M, Nov’2017)

26. Demonstrate the procedure for obtaining product-of-sums using k-maps? (8M, Nov’17)

27. What is the role of Processor clock, clock rate in the performance of computer system? Explain. (7M, Apr’18)

28.a)Role of MDR in fetching a word from memory. (4M -, Apr’2018)

29. c) Block diagram of a complete processor . ((5M, Apr’2018)

30. What is the use of pipelining and superscalar operations? (3M, Apr’18)

UNIT-2: Machine Instruction and Programs

1. What do you mean by register transfer language? What are the uses of register transfer language? (4M, Nov’17)

2. Describe the phases of instruction cycle briefly. (5M, Nov’17)

3. What are the basic differences among a branch instruction, a call subroutine instruction, and program interrupt? (8M, Nov’17)

4. Write short notes on additional addressing mode. (2M, Apr’18)

5. Describe the basic Instruction format. (4M, Nov’17)

6. Construct a bidirectional shift register with parallel load and give the function table of the circuit.(OS) (8M, Nov’17)

8. An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow? (8M, Nov’17)

10. Using a 4-bit counter with parallel load and a 4-bit adder, draw a block diagram that shows how to implement the following statements:

x: R1 ←R1+R2 Add R2 to R1

x ' y: R1← R1+1 Increment R1

where R1 is a counter with parallel load and R2 is a 4-bit register. (8M, Nov’17)

11. Explain the functionalities and applications of the following

i. Decoders ii. Encoders iii. Multiplexers iv. De-multiplexers (8M, Nov'17)

12. Differentiate the instruction execution for adding 'n' numbers using Straight line sequencing and branching? (7M, Apr'18)

13. Write short notes on shift and rotate instruction. (7M, Apr'18)

14 a) Write about various means by which data are transferred between memory of a computer and outside world. (7M, Apr'18)

b) Write the subroutines for parameter passing through registers. (7M, Apr'18)

15 a) What is register transfer notation? Write and explain these notations to three-address, two-address, single address and zero-address instruction types. (7M, Apr'18)

b) llustrate the concept of assembly directives with an assembly language Program. (7M, Apr'18)

16. Give example for left and right shift operations. (2M, Apr'18)

17. In how many ways the location of an operand is specified in an instruction? Explain each mode with suitable examples. (14M, Apr'18)

18. Represent the number $(+46.5)_{10}$ as a floating-point binary number with 24 bits? The normalized fraction mantissa has 16 bits and the exponent has 8 bits? (8M, Nov'17)

19. Distinguish between fixed point representation and floating point representation.

(8M, Nov'17)

20. Describe fixed point representation and floating point representation? (8M, Nov'17)

21. Illustrate with examples fixed point representation and floating point representation

(8M, Nov'17)

22. List basic input and output operations. (2M, Apr'18)

23. Explain 3 steps a processor perform to execute instruction (2M, Apr'18)

Unit -3 :type of Instructions

1. Give the flow chart of addition and subtraction of two floating-point binary numbers.

(8M, Nov'2017)

3. What are addressing modes? Give an overview of the addressing modes.

(8M, Nov'2017)

4. With an example write about relative addressing. (2M, Apr'18)

5. Differentiate post-indexed and pre-indexed addressing with write back policy. (3M, Apr'18)

6. Suppose two numbers located in memory are to be added. What are the functional units of digital computer system will carry out this? Explain how. (7M, Apr'18)

UNIT-4 :Input/Output Organization

1.Give few examples of external interrupts and few examples of internal interrupts. What is the difference between a software interrupt and subroutine call? (8M, Nov'17)

2. What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? (5M, Nov'17)

3. Define cycle stealing. (3M, Nov'17)

4. What do you mean by vectored interrupt? (2M, Apr'18)

5. What is bus arbitration? (2M, Apr'18)

6 Write about the transfer of control between programs through interrupts.

(3M, Apr'18)

7. What is the use of PCI bus in a computer system? (2M, Apr'18)

8. Discuss various types of Interrupts. (4M, Nov'17)

13. Demonstrate how communication proceeds between CPU and IOP?. (8M, Nov'17)

14. Explain in detail various I/O modes of transfer. (8M, Nov'17)

15. Design parallel priority interrupt hardware for a system with eight interrupt sources.

(8M, Nov'17)

16. What is direct memory transfer? Give an overview and the block diagram of a DMA controller. (8M, Nov'17)

17. Demonstrate interrupt-initiated I/O. (8M, Nov'17)

18. Explain the functionalities of an IOP interface unit. (8M, Nov'17)

19. Give an overview of parallel priority interrupt hardware. (8M, Nov'17)

20. Demonstrate the mechanism of DMA. (8M, Nov'17)

21. Explain typical read operation with various data transfer signals on the PCI bus.

(7M, Apr'18)

22. Write about two different approaches for bus arbitration. (7M, Apr'18)

23. What are the main phases involved in the operation of SCSI bus? (7M, Apr'18)

24. List the functionalities of I/O interface. Draw and explain a combined input/output interface circuit?

25. Discuss the implementation of nested interrupts to handle multiple devices?

(7M, Apr'18)

26. Explain the importance of handshake control for data transfer in asynchronous bus?

(7M, Apr'18)

27. How to meet device characteristics and addressing objectives by USB? (7M, Apr'18)

28. Explain the usage of daisy chains and priority in simultaneous interrupt handling? (7M, Apr'18)

UNIT-5: Memory Systems

1. What is the purpose of cache memory? (3M, Nov'17)

2. What do you mean by content addressable memory?(OS) (3M, Nov'17)

3. What do you mean by bootstrap loader? (OS) (4M, Nov'17)

4. What do you mean by associative memory? Give applications of associative memory.(OS)

(5M, Nov'17)

5. Explain the functionalities of memory management hardware.(OS) (8M, Nov'17)

6. Explain various mapping procedures of cache memory with an example.

(8M, Nov'17)

7. A computer employs RAM chips of 256×8 and ROM chips of size 1024×8. Extend the memory system to 4096 bytes of RAM and 4096 bytes of RAM. List the memory address map and indicate what size decoders are needed? (8M, Nov'17)

8. Demonstrate with an example address mapping using pages?(OS) (8M, Nov'17)

9. Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 μs; level 2 contains 1,00,000 words and has an access time of 0.1μs. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose, we ignore the time required to determine whether the word is in level

1 or level 2 and 95% of the memory accesses are found in the cache, then what is the average access time of a word? (OS) (8M, Nov'17)

10. Write the instruction format of ARM? (OS) (2M, Apr'18)

11. What is cache memory? What are its advantages? Explain?. (8M, Nov'17)

12. Demonstrate logical to physical address mapping using segmented-paging.(OS)

(8M, Nov'17)

13. What is virtual memory? Explain .(OS) (8M, Nov'17)

14. Write about flash memory and read only memories. Explain their applications.

(7M, Apr'18)

15. Write about locality of preference, write-through protocol, copy-back protocol and early restart protocol in cache memory.

(7M, Apr'18)

16. Explain how large storage can be implemented with optical disks (7M, Apr'18)

17. Discuss the possible methods for specifying the placement of memory blocks in cache.

(7M, Apr'18)

18. Differentiate static and dynamic RAMs. (2M, Apr'18)

19. Relate the access speed, size and cost of various memories in memory hierarchy system. (7M, Apr'18)

20. Write the major functionalities of disk controllers (OS) (3M, Apr'18)

21. "RAID disks offers excellent performance and large & reliable storage"- Justify this statement through various levels? (OS) (7M, Apr'18)

22. Explain the following: (5M + 4M + 5M, Apr'2018)

a) Storing a word in memory.

b) Basic operation of micro programmed control unitc) Input and Output gating of ALU23. Differentiate logical and physical addresses. (2M, Apr'18)

24. What are the possible configurations of ROM? Explain with advantages and disadvantages. (7M, Apr'18)

25. Write about organization accessing of data on a disk. Elaborate the role of operating systems and disk controllers in it. 7M, Apr'18)

UNIT-6: Processing Unit

1. Define Micro-operation. (4M, Nov'17)

2. Define micro program. (3M, Nov'17)

3. Define Microcode. (3M, Nov'17)

4. Explain basic organization of micro programmed control unit. (3M, Apr'18)

5. Define Microinstruction. (3M, Nov'17)

6. How to determine branch target address? (2M, Apr'18)

7. What is micro programmed control and micro routines? (2M, Apr'18)

8. Discuss load/store instructions for multiple operands. (3M, Apr'18)

9. Write short notes on wide-branch addressing. (3M, Apr'18)

10. Give an overview of address sequencing in micro programmed control unit.

(8M, Nov'17)

11. Formulate a mapping procedure that provides eight consecutive microinstructions for each routing. The operation code has six bits and the control memory has 2048 words.

(8M, Nov'17)

12. Distinguish between micro programmed and hardwired control unit. (8M, Nov'17)

13. What are the microinstructions needed for the fetch routine? Explain. (8M, Nov'17)

14. a) What are main types of control units? Explain briefly. (8M, Nov'17)

b) Give the block diagram of a control memory and the associated hardware needed for selecting the next micro-instruction address. (8M, Nov'17)

15. a)What is the difference between a microprocessor and micro program? Is it possible to design a microprocessor? (8M, Nov'17)

b) Explain, how address sequencing is done in a micro programmed control unit?(8M, Nov'17)

(7M, Apr'18)

Processor design

1. Write about Pipeline conflicts. (4M, Nov'17)

2. Illustrate arithmetic pipeline with an example.(OS) (8M, Nov'17)

3. Derive speedup achieved by a pipeline unit over a non-pipeline unit. (8M, Nov'17)

4. What are the pipeline conflicts that cause the instruction pipeline to deviate from?(OS) (8M, Nov'17)

5. Illustrate with an example an instruction pipeline (OS). (8M, Nov'17)

7. Block diagram of a complete processor.

8. Write about delayed branch.(OS) (3M, Nov'17)

9. What do you mean by delayed load?(OS) (2M, Nov'17)

10. Describe about MIMD. (OS) (3M, Nov'17)

12. Explain about the following: (5M + 5M + 4M, Apr'2018)

a) Conditional branching micro program

b) Vertical/Horizontal organization of micro instruction.

c) Fetching a word from memory.

13. How to encode bits using Manchester encoding? (OS) (2M, Apr'18)

14.. Explain about the following: (4M + 5M + 5M, Apr'2018)

a) Single bus organization of the data path inside a processor.

b) Micro program sequencing.

c) Micro instructions with next address field

15. b) Control sequence that implements unconditional branch instructions (5M ,Apr'2018)